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High speed low power FEE for silicon detectors in nuclear physics applications

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ABSTRACT

A high speed, low power and programmable readout front-end system is presented for silicon detectors to be used in nuclear physics applications. The architecture consists of a folded cascode charge sensitive amplifier, a pole-zero cancellation circuit to eliminate undershoots and a shaper circuit with Gm-C topology. All building blocks include a regulated cascode technique based gain enhancement. Experimental results show that the whole front-end system can be programmed for peaking times of 100 ns, 200 ns and 400 ns maintaining the amplitude of the output voltage. Programmability is achieved by switching different resistors for all poles and zeros. The system has been designed in a 130 nm CMOS technology and powered from a 1.2 V supply. The output pulse has peak amplitude of 200 mV for an input energy of 5 MeV from the detector. A power consumption low noise tradeoff will be considered.

1. Introduction

Silicon surface-barrier detectors are extensively used for photon-counting imaging systems in medicine [1–4] and for modern charged particle detection arrays in nuclear and particle physics [5–7]. These devices take advantage of the unique properties of high-resolution pixellized silicon detectors developed in the last decade. They are reverse-biased diodes that release charge towards its electrodes when exposed to ionizing radiation. The energy deposited in these detectors is converted to an electric signal. For measuring the deposited energy, which is proportional to the integrated current signal, a readout electronics system, also called front-end electronics (FEE), is required.

Highly pixellized silicon detectors have been used in high-energy physics (HEP) experiments for tracking applications (ranges of signals up to 20 fC max) and in nuclear medicine and biology (gammas up to 500 keV). Front-end electronics with large dynamic range (10 MeV) has been recently used in calorimeter detectors for HEP applications, as in the pre-shower detector of the CMS experiment at CERN/LHC accelerator (Geneva, Switzerland). On the other hand, the new generation of nuclear physics silicon detector arrays for the new Radioactive Beam facilities like GES/FAIR (Darmstadt, Germany), GANIL/SPIRAL2 (Caen, France) and LNL/SPES (Legnaro, Italy) are extremely demanding in terms of detector performance and large dynamic ranges (from few MeV up to several GeV) and timing properties down to the pico-second resolution, pushing the silicon detector technology to the physical limits. There are a number of transnational collaborations bringing experts to collaborate in new low-energy particle detection systems like GASPARD (SPIRAL2), HYDE (FAIR) and TRACE (SPES). An R&D program has been settled for the production of prototype silicon detection systems based on the use of thick silicon wafers where low energy heavy ions, in the range of 1–50 MeV/u must be fully stopped in segmented silicon wafers, collecting full energy and charge current flow (pulse shape) information with highest resolution to extract the relevant nuclear structure and nuclear reaction information. For this purpose great research efforts are being carried out on the development of specific state-of-the-art FEE for these nuclear physics applications. [8–12].

There are several specifications to be considered in the design of a valid FEE system. The preamplifier stage must be as close as possible to the detector to minimize inductance effects and spurious capacitance from the connection load. For most applications this feature obliges designing a minimum power consumption device, as the diodes are normally placed in vacuum or in a tightly closed environment. On the other hand, typical diode capacitances for nuclear physics applications vary nearly by one order of magnitude in the range of 20–200 pF. Therefore the goal of achieving a low noise low power FEE device with the final energy resolution better than 0.1% needed for spectroscopy applications becomes an important technological challenge.

Traditionally discrete and hybrid electronics are used for the readout front-ends in semiconductor detector systems for nuclear spectroscopy applications. These approaches are inadequate for

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high density and increased number of channels demanding low power, low noise and small area. The continuing down-scaling of CMOS processes has led to the implementation of readout front-end systems with multichannel architecture where analog and digital circuits are on the same chip. One significant challenge for analog designers is achieving low noise for high speed front-end systems, while at the same time minimizing the power consumption as much as possible [13–17]. The noise of the front-end is a function of the detector capacitor, leakage current, shaping time, and allowed power dissipation.

This paper aims to contribute to this trend proposing circuit solutions to overcome the drawbacks for analog design in modern technologies related to low intrinsic gain of transistors. Owing to at architectural level the conditioning electronics for the front-end readout systems is known, this work is focused on the implementation of the building blocks of the chain using gain-boosting techniques. These techniques are needed to achieve the open-loop gain for these blocks, but the low voltage environment limits the number of stacked transistors in each branch, and low power consumption demands circuit simplicity. The paper is laid out as follows: Section 2 describes the building blocks of the readout front-end system. Section 3 discusses design considerations and shows experimental results. Finally, in Section 4 conclusions are drawn.

2. Description and design of the readout system

Fig. 1 shows the analog part of the channel basic architecture of the readout front-end system for this kind of detector. The first component in the chain is the detector together with the type of biasing. The detector is a capacitive device with high impedance and weak output signal. The detector delivers a charge that is amplified and shaped in the front-end electronics. An operational amplifier based integrator with a feedback capacitance is commonly used due to the gain is insensitive to the detector capacitance C_{det}. The function of this amplifier, called "charge sensitive amplifier" (CSA), is to integrate the weak charge pulses produced by the detector and convert them into voltages pulses. The generated charge is integrated into a small feedback capacitor C_F. The CSA's output is a voltage step with amplitude proportional to the charge generated in the detector. This voltage pulse then slowly discharges by the feedback resistance R_F connected in parallel to C_F. Usually the value of the resistance needs to be adjusted to control the decay time and prevents the saturation of the stage in case of high rate of incoming current pulses. The voltage step is fed to a shaper (band pass filter), which provides pulse shaping according to timing requirements and filters noise to maximize the signal to noise ratio. The shaper consists of a high pass section followed by several integrators. The CSA is dc coupled to the shaper. The pole-zero cancellation (PZC) circuit avoids the undershoot produced by the pole of the CSA at the shaper's output.

2.1. Charge sensitive amplifier

This preamplifier is the critical block of the readout front-end system. In general, the design of the CSA requires as main characteristics low noise, low power consumption, high open-loop gain, high gain-bandwidth (GBW) product and fast rise time. A careful design for the input transistor is mandatory for low noise and optimum power consumption.

The rise time of the output voltage should be smaller than the integration time of the charge over the feedback capacitor. The time constant $\tau_F = R_F \cdot C_F$ is responsible for slow signal decay and GBW determines the rise time at CSA output. Thus, in order to transfer quickly the charge generated by the detector to the preamplifier, the GBW must be sufficiently large. Furthermore, a high open-loop gain of the circuit ensures that the output is independent of the detector capacitor.

Telescopic, two-stage Miller and folded cascode topologies with single-ended input and single-ended output are the most commonly solutions for CSA. Folded cascode topology is a single gain stage but with a quite reasonable gain achieved by the product of the input transconductance and the high output impedance due to the use of cascode techniques. The bandwidth is proportional to the input transistor's transconductance. To enlarge the transconductance the bias current of the input transistor should be several times larger than the bias current of the output branch. This approach optimizes the power consumption further increasing the output resistance, and thus the dc gain ($g_{mi} \cdot r_{out}$). The very large transconductance of the input transistor reduces the thermal noise.

Until few years ago, the design of CSA in CMOS technologies of 0.35 μm o larger easily provided high open-loop gain where the transistor's intrinsic gain factors g_m/g_{ds} were relatively large. Currently, gain enhancement techniques in combination with low voltage techniques are required to overcome the low intrinsic gain limitation in fine line technologies. In addition, analog circuits only benefit marginally by the scaling down of the technology because minimum size transistors cannot be used due to noise requirements. The low supply voltage complicates the design requiring very efficient topologies that combine low-voltage operation with high power efficiency and small die area. Cascode output stages take away a large fraction of the output signal swing which is already severely limited by the low supplies used. In order to prevent severe signal swing limitation, analog circuits with low supply voltages require transistors operating with small

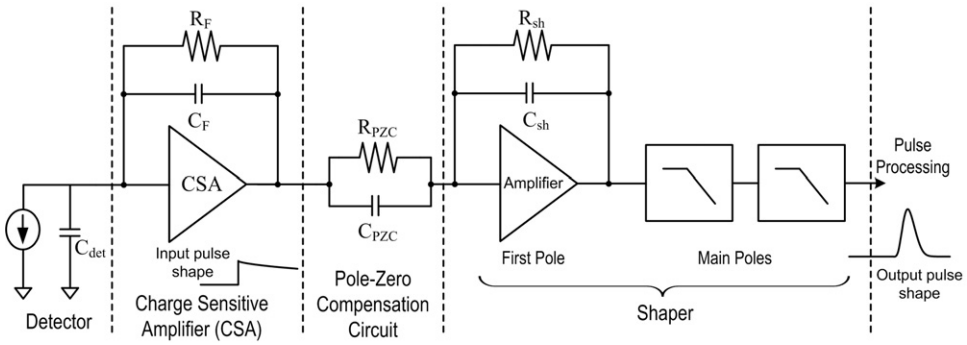

Fig. 1. Architecture of the designed front-end readout system. It shows the analog part of the channel basic architecture of the readout front-end system for this kind of detector.