Nuclear Instruments and Methods in Physics Research A 697 (2013) 17–22

Contents lists available at SciVerse ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

The status and improvement of the HIRFL-CSR operation software

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ARTICLE INFO

Article history:
Received 10 May 2012
Received in revised form
6 September 2012
Accepted 6 September 2012
Available online 14 September 2012

Keywords:
HIRFL-CSR
Accelerator control
Timing system
Operation software

ABSTRACT

HIRFL-CSR is a new ion cooler-storage ring system in China's Institute of Modern Physics (IMP). This facility can accelerate all ions from protons up to the heaviest element, uranium, with variable energies for nuclear physics experiments, material irradiation research, and heavy ion particle therapy and so on. With the completion of this project, a new accelerator control system has been developed to accomplish the beam injection, accumulation, acceleration, extraction and manipulation. In this paper, the architectures of the HIRFL-CSR control system and timing system, the basic function of operation software, the data cycles of power supplies and the RF cavity are described in detail. Furthermore, to fulfill the requirements of special physics experiments and enhance the facility reliability, several operation software improvements, including eliminating the magnetic hysteresis effects, dipole magnets field slow feedback and super-period slow extraction, are also introduced in this paper.

1. Introduction

The HIRFL-CSR system consists of the main cooler-storage ring (CSRm), RIB production and transfer line two (RIBLL2), experimental storage ring (CSRe) and experimental terminals. The two existing cyclotrons, the Sector Focus Cyclotron (SFC) and Separated Sector Cyclotron (SSC), at the Heavy Ion Research Facility in Lanzhou (HIRFL) are used as the injector system. The heavy ion beams from HIRFL are injected into the CSRm and then accumulated, e-cooled and accelerated before being extracted to the CSRe for internal target experiments and other physics experiments [1]. Fig. 1 shows the overall layout of the HIRFL-CSR. Until now, the HIRFL-CSR has succeeded in accumulating and accelerating particles from protons to uranium ions and providing different beams for physics experiments such as the radioactive electron capture (REC) experiment, Isochronous Mass Spectrometer (IMS) precise mass measurements in the CSRe and particle therapy experiments [2].

2. Architecture of the control system

The HIRFL-CSR control system is a distributed network control system that has three hierarchical layers of equipment communicating through the HIRFL-CSR technical network, a gigabit Ethernet network using the TCP-IP protocol. The HIRFL-CSR accelerator control system architecture is illustrated in Fig. 2. The first layer consists of applications for operators and end-users. Typically, these are graphical user interface (GUI) applications, but they can also be web applications or command-line scripting tools. The second layer contains the controllers of different devices that provide communication between the users and the end devices. The controllers, which consist of AT91RM9200 (ARM) controllers and Digital Signal Processors (DSPs), are completely designed, commissioned, developed and implemented by the Institute of Modern Physics (IMP) control group. The Component Object Module (COM) running on the Front Sever (FS) is responsible for distributing the data and event sequences to the ARM controllers and DSPs. The DSPs are connected to the timing system network and transfer data to devices according to the event sequences that are distributed by the timing system. The third layer contains power supplies, beam position monitors, vacuum instruments and so on. A relational database management system, ORACLE 10g, runs on the server workstation and stores all information relevant to the HIRFL-CSR, including the machine parameters, equipment specifications and multi-energy data for particle therapy [3–5].

3. Timing system

The primary task of the timing system is to trigger and synchronize equipment actions, which are timed according to the accelerator cycles, and to synchronize devices that must operate simultaneously [6]. A virtual-accelerator concept that organizes the data for different accelerator cycles is adopted in the control system. The timing system of the HIRFL-CSR is based on an event

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http://dx.doi.org/10.1016/j.nima.2012.09.015

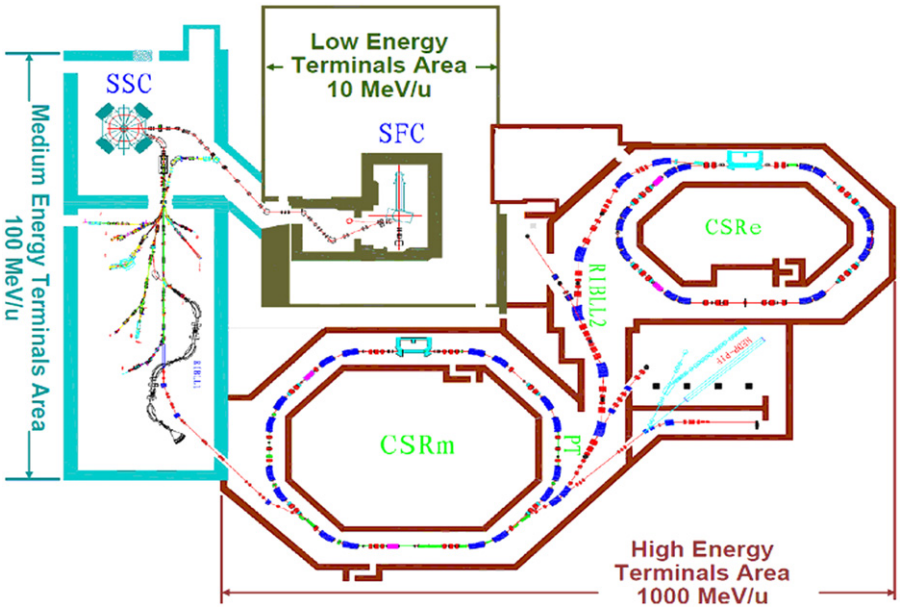

Fig. 1. The overall layout of HIRFL-CSR.

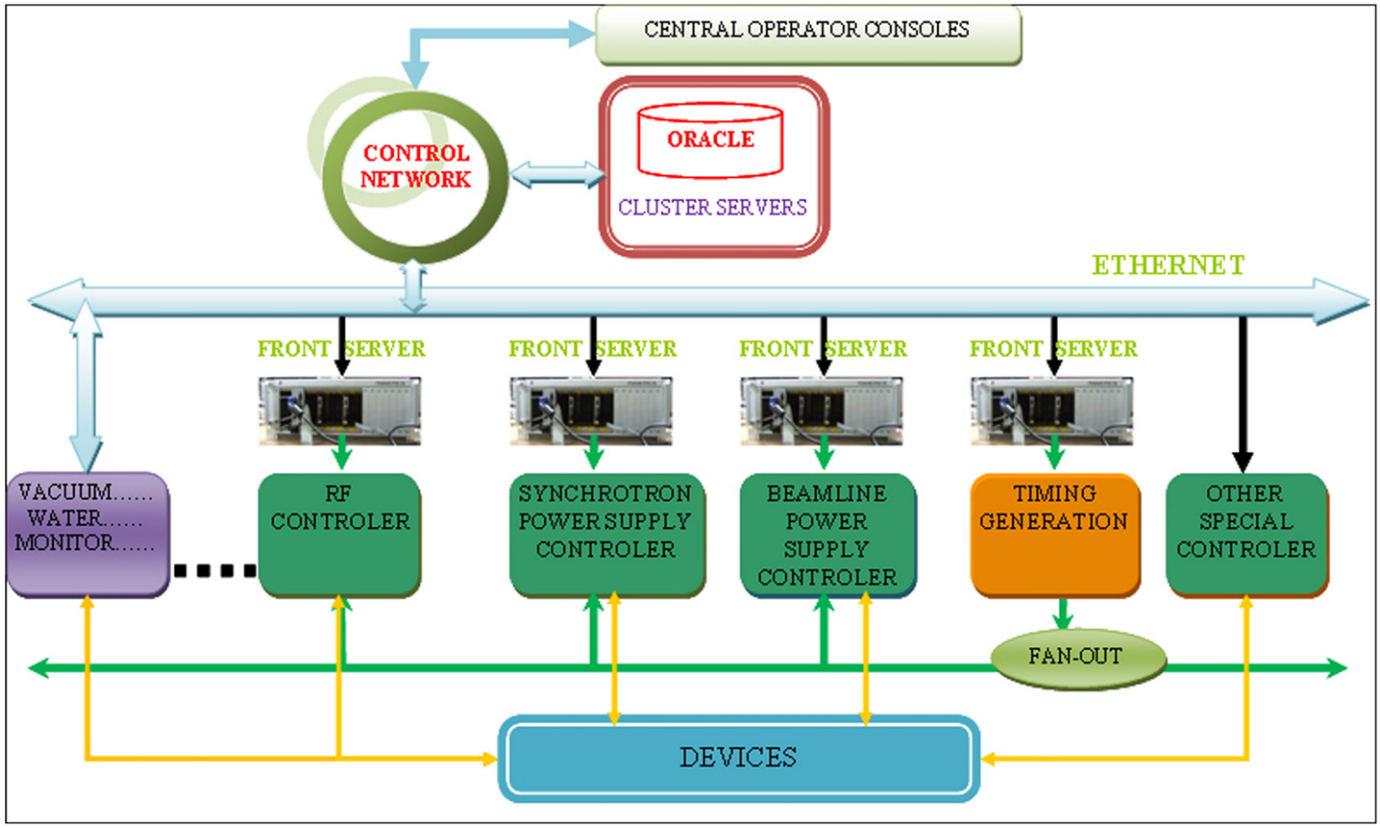

Fig. 2. Architecture of the HIRFL-CSR accelerator control system.

distribution system that broadcasts the timing information to all components for synchronization [7]. The timing system scheme is illustrated in Fig. 3. The whole operation cycle is generated within the Event Generator (EVG), which is a PCI bus card inserted into a synchronous server. The EVG sends 32-bit event codes over an optical network, and the bit stream is distributed to several branches with fan-out modules. The Event Receiver (EVR), which resides in the DSPs, decodes the event stream and provides hardware outputs or software interrupts based on event information. All event codes of a device are stored in an event file which is structured as follows: event sum, event 1, delay 1, event 2, delay 2,…, event *n*, delay *n*, output trigger pulse width [7,8].

4. Operation software

The HIRFL-CSR operation software can be divided into two parts: the HIRFL operation software based on the former control