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The power supply system for the DEPFET pixel detector at BELLE II

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ABSTRACT

The upgrade of the KEKB accelerator towards 8×10^{35} cm^{-2} s^{-1} poses several challenges for the BELLE II detector. Especially the innermost detector will be faced with a significant radiation of several MRad per year as well as a high hit density. To cope with this a silicon pixel detector will be used for the inner layers of the silicon tracker.

The pixel detector (PXD) consists of two layers of DEPFET active pixel sensors. The DEPFET technology has an unique set of advantages like low power dissipation in the active area, flexible device size, radiation hardness and a thinning procedure allowing to adjust the thickness of the device over a wide range. The two layers close to the interaction point together with a low material budget will improve the IP resolution by a factor of 2 compared to the previous installed silicon detector. In addition silicon stand-alone pattern recognition will be possible together with the four layers of double sided strip detectors (DSSD) of the strip detector.

The PXD detector system consists of the DEPFET modules with integrated readout chips, the data handling hybrid receiving the data and sending them to compute nodes performing an online pattern recognition. Moreover the power supply system provides the supply voltages for the DEPFET from a position outside of the detector. The power distribution is designed to provide low output impedance over all frequencies and transient response with appropriate overshoots. The PXD pose several challenges to the power distribution system—number of voltages, tight requirements on regulation and noise.

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1. Introduction

The upgrade of the KEKB accelerator towards a luminosity of 8×10^{35} cm^{-2} s^{-1} is an improvement of a factor of 40 compared to the previous KEKB machine [1]. The physics program at the SuperKEB facility is centered around the investigation of CP violation in the $B\bar{B}$ system, the investigation of rare decays as well as hadron physics.

The new accelerator will allow to measure CP violation in the $B\bar{B}$ system with unprecedented precision. The improvements will constrain the unitarity triangle and eventually put light on physics beyond the standard model by identifying tensions in the triangle. Besides rare decays like $B \rightarrow \tau\nu$ will be accessible. An integrated luminosity of 40 ab^{-1}, expected for SuperKEKB, will allow to probe new physics in this channel into the multi TeV range [2].

However the luminosity will pose several challenges for the detectors. Especially the innermost detector will be faced with an increased hit rate which makes the use of silicon strip detectors difficult as the occupancy would make pattern recognition impossible.

To cope with this issue a two layer pixel detector based on the DEPFET technology will be installed. Together with four layers of double sided strip detectors of the SVD [3] six layers silicon will be available.

2. The BELLE II pixel detector

The DEPFET detector is an active pixel sensor with in-pixel amplification. The DEPFET pixel consists of a p-channel MOS-FET integrated on a fully depleted silicon bulk. The absence of external connections allows to build an amplifier with minimal input capacitance in the order of 30 fF and low intrinsic noise [4].

To obtain a good impact parameter (IP) resolution the detector should be as close as possible to the interaction point, have good point resolution and minimal material. Table 1 gives an overview

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of the detector layout, a drawing of the assembled detector is depicted in Fig. 1.

Currently a comprehensive research and development effort is ongoing. Topics like ASIC development [5], thermal management and mechanics [6] and test beam measurements [7] will not be covered here but can be found in the mentioned publications.

Pixel cell: Simulation showed that the optimal pixel size which gives a fair balance between readout speed and resolution is 50 μm^2 in the inner and $50 \times 75\ \mu m^2$ in the outer layer. To assure a high charge collection efficiency an additional implant to provide a lateral electrical field from the exterior of the pixel towards the internal gate has been introduced. A typical layout is shown in Fig. 1 the picture shows a single cell containing two pixels.

Thinning technology: As the DEPFET is a double sided detector the thinning technology must preserve the quality of the backside. A thinning technology compatible with the DEPFET process has been developed and allows to tailor the thickness of the active area between 50 μm and 450 μm thickness. The modules are self-sustained and need no further mechanical support, details can be found in Ref. [8].

Readout: The readout of the matrix is done in rolling shutter mode. The readout is performed in the following way—a row is activated, the current of each pixel is digitized and a reset pulse is applied. Three different chips are involved in the readout process: the Drain Current Digitizer (DCD) which incorporates an transimpedance amplifier and a 8 bit ADC for the digitization, the Switcher chips for applying the row select and reset pulses and the Data Handling Processor (DHP) where common mode, pedestal corrections and finally as a zero suppression is performed [5]. The synchronization of the readout process is done on the DHP, too. To reach the frame time of 20 μs a row processing time of ≈ 100 ns is required.

System layout: The layout of the DEPFET PXD system is depicted in Fig. 2. The data generated by the module is transmitted with four differential links via the 40 cm flex circuits—the Kapton flex—and the 15 m twisted pair cable to the Data Handling Hybrid (DHH). The DHH performs serialization of the data into a optical fiber and send them to the compute nodes. In addition the DHH distributes the trigger and synchronization

of the accelerator to the detector. That data rate at the DHH is still dominated by hits created by background like synchrotron radiation, intra beam scattering, beam gas interaction and QED backgrounds. The compute nodes will receive not only the PXD data but also data from the SVD and the drift chamber. Using this information a further reduction of the data rate is possible by performing an online pattern recognition allowing rejecting the background hits from the PXD data stream.

Cooling: In total around 400 W of heat must be removed during operation of the pixel detector. The power dissipation is dominated by the readout chips. The large size of the DEPFET module allows placing the readout chips outside of the acceptance region. With this the mass within the acceptance is not further increased. The thermal management is performed in a twofold way: Within the acceptance region cooling with cold air [6] is foreseen. In addition to this active cooling using CO_2 is foreseen. The mechanical support of the pixel detector serves as cooling block with direct thermal contact to the detector modules.

Performance: Detailed simulation studies have been performed to optimize the layout of the PXD. The figure of merit of the vertex detector is the impact parameter resolution. The parameters given in Table 1 lead to the impact parameter resolution displayed in Fig. 3. In case of high p_t the impact parameter resolution along the z-axis is improved by a factor of 2 compared to the silicon detector used at Belle. At lower energies the resolution improves even more thanks to the low material present in the detector.

3. Power supply and distribution system

An essential part of the PXD detector is the power supply system and the power distribution. Both systems must be designed in a way that allows the detector to work close to its nominal performance. The first part of the section gives an overview of the requirements on the power supply units and the second on the recent developments in this area.

3.1. Requirements

As described in Section 2 a detector module comprises the DEPFET matrix, the Switcher chips, the frontend chip DCD and the DHP chip. All of them need dedicated supply voltages. In total 22 voltages must be supplied to each detector module. In addition there are several dependencies between the voltages which must be controlled. The most important requirements to the power supply voltages are

- Noise $\approx 1\ mV_{rms}$.
- Settable hardware current limits.

Table 1
PXD in a nutshell.

Parameter	Layer 1	Layer 2
Radius	14 mm	22 mm
Pixel size	$50 \times 50\ \mu m^2$	$50 \times 75\ \mu m^2$
Module size	$136 \times 12.5\ mm^2$	$169 \times 12.5\ mm^2$
Thickness	75 μm	
Frame time	20 μs	
Material budget	$0.2\% X_0$	
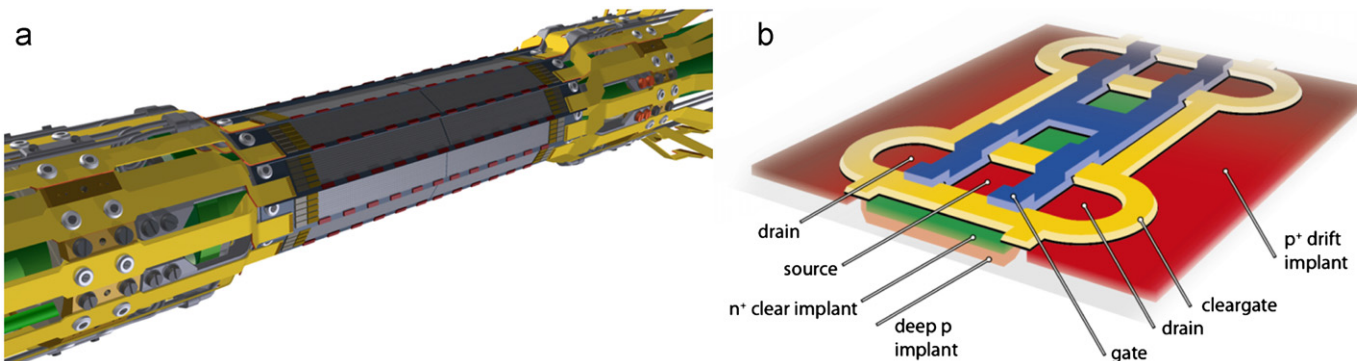
Fig. 1. (a) Drawing of the assembled pixel detector, (b) shows the layout of the BELLE II DEPFET pixel design.