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Overview of the ATLAS insertable B-layer (IBL) project

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ABSTRACT

The upgrades for the ATLAS Pixel Detector will be staged in preparation for high luminosity LHC. The first upgrade will be the construction of a new pixel layer which will be installed during the first shutdown of the LHC machine, foreseen in 2013–2014. The new detector, called the Insertable B-layer (IBL), will be installed between the existing Pixel Detector and a new, smaller radius beam-pipe at a radius of 3.3 cm. The IBL will require the development of several new technologies to cope with increased radiation and pixel occupancy and also to improve the physics performance through reduction of the pixel size and a more stringent material budget. Two silicon sensor technologies, planar and 3D, are currently under investigation for the IBL. An overview of the IBL project, of the module design and the qualification for these sensor technologies is presented.

1. Introduction

The ATLAS [1] Inner Detector (ID) [2] provides charged particle tracking with high efficiency. The innermost sub-system of the ID is the Pixel Detector [3] which consists of three cylindrical barrel layers between 50 and 120 mm around the beam axis and three forward and backward endcap disks. The Pixel Detector significantly enhances track impact parameter resolution, and therefore, vertex reconstruction and *b*-tagging. To further improve the performance of the silicon system and to compensate possible deterioration that the innermost layer of the Pixel Detector may suffer after the first few years of operation, ATLAS will insert an additional pixel layer (Insertable B-Layer or IBL [4]) inside the current Pixel Detector during the LHC shutdown planned for 2013–2014. To improve the physical performance the material budget of the IBL has to be kept to a minimum.

The IBL baseline design consists of 14 staves mounted directly on a new, smaller, beam pipe with a tilt angle of 14° (see Fig. 1). The average radius of the sensitive area is 3.3 cm. Each stave is equipped with 16 to 32 modules depending on the final sensor layout. Two sensor technologies are currently under investigation for the IBL modules, planar and 3D sensors. Planar modules are interconnected to two front-end chips doubling their length in the *z* direction with respect to the 3D modules, which are read out by a single chip. A stave layout being considered combines planar and 3D sensors (in the forward region). The IBL design foresees a material budget of $X/X_0 = 1.5\%$ at $z = 0$ cm including all support structures. Due to space restrictions the IBL modules will have no overlap in the *z* direction, making imperative the need of very small inactive edges to minimize efficiency losses.

The IBL will have to sustain high radiation doses until the replacement of the entire Inner Detector for the high luminosity LHC (foreseen around 2020). The IBL design assumes an integral luminosity of 550 fb^{-1} and a peak luminosity of 3×10^{34} cm^{-2} s^{-1} to determine the sensor requirements. Including conservative safety factors, this translates into a non-ionizing energy loss (NIEL) dose of 5×10^{15} n_{eq}/cm^2 (where n_{eq} represents a particle with the non-ionizing energy loss of a 1 MeV neutron) and an ionization dose of 250 Mrad. Up to this fluency, IBL modules are required to provide a hit efficiency in the active area $> 97\%$. Other constraints to achieve this efficiency are the operational temperature, set at -15 °C, and the maximum bias voltage, set at 1000 V. The power dissipation should not exceed 200 mW/cm^2 at the nominal temperature. Finally, the sensor design has to minimize the dead regions, in order to achieve this both planar and 3D sensors target inactive edges of 200 μm.

2. The front-end chip for the IBL

To cope with the radiation and high occupancy environment of the inner radii of the ATLAS ID, the front-end readout electronics and the sensor technology used in the present Pixel Detector have to be upgraded. The readout chip used in the present detector, the FE-I3 [5], was excluded from the IBL design because its active footprint is too small and its hit rate capability is not high enough [4]. The IBL will utilize the FE-I4 integrated circuit [6], which was designed in 130 nm technology and features an array

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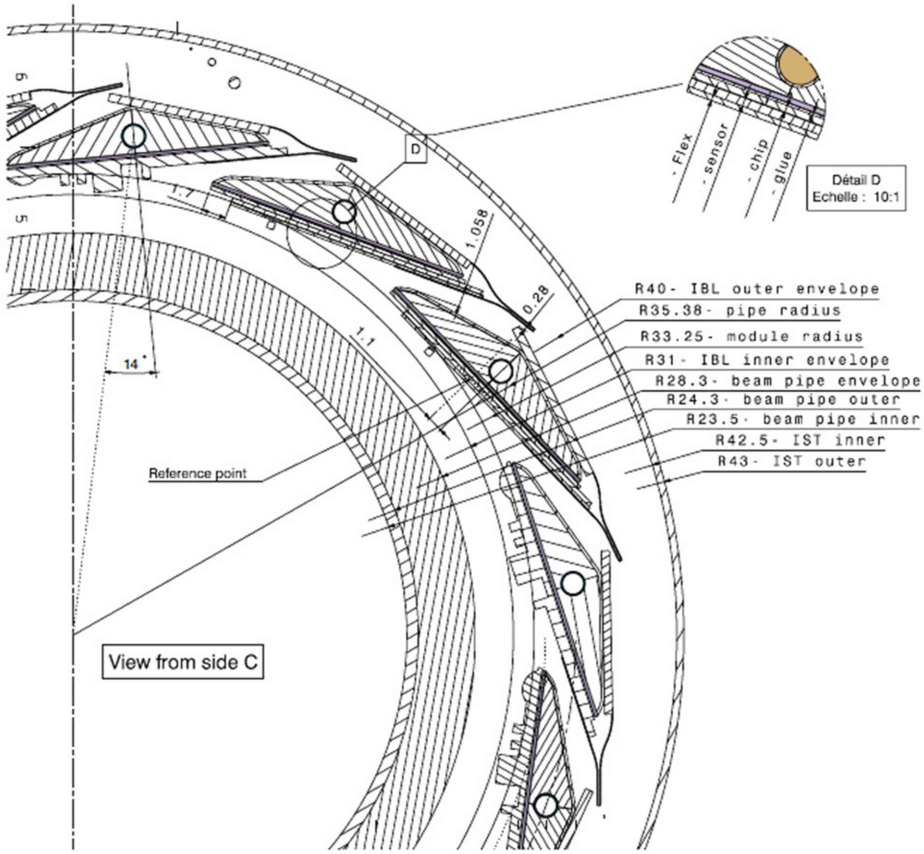

Fig. 1. Cross-section detail of the IBL, beam pipe and IBL support tube (IST). Distances are given in mm.

of 80 × 336 pixels with a pixel size of 50 × 250 μm^2. The large size of the chip, 20.2 × 19.0 mm^2, leads to a larger active fraction than its predecessor (89% vs 74%). The sensors are DC coupled to the chip with negative charge collection. Each readout channel contains an independent amplification stage with adjustable shaping, followed by a discriminator with independently adjustable threshold. The chip operates with an externally supplied clock, nominally at 40 MHz. The time over threshold (ToT) with 4-bit resolution together with the firing time are stored for a latency interval until a trigger decision is taken. The primary output rate is 160 Mb/s, four times faster than the output rate of the FE-I3 chip. The first prototype of the chip (FE-I4A) has been submitted in 2010 and studied with and without sensors, before and after irradiation, in laboratory and beam tests (see Section 7).

3. Pixel sensors for the IBL

Planar modules consist of 2-chip assemblies while 3D modules consist of a single chip. Both module designs offer similar nominal acceptance. However, the requirements of the two technologies in terms of temperature and bias voltage differ, being less restrictive for 3D sensors. Both technologies have to demonstrate that they satisfy the IBL requirements in terms of performance after irradiation to 5×10^{15} n_{eq}/cm^2. Planar and 3D sensors with the IBL design have been fabricated, and interconnected (bump-bonded) with the FE-I4A read out chip. These planar and 3D bare assemblies were wire-bonded to an electronic card to carry out the characterization and test-beam studies needed to evaluate the technologies.

3.1. Planar sensors

The IBL planar sensors are based on the proven technology of the current ATLAS Pixel Detector [7], n-on-n pixels on a diffusion oxygenated float-zone silicon bulk. The chosen thickness for the substrate is 200 μm, a sizable reduction from the 256 μm featured in the current Pixel Detector. Isolation between the n^+ implants is obtained through the moderated p-spray technique. A bias grid [7] is integrated into the design to determine the sensor electrical quality before bump-bonding. In order to reduce the inactive edges, the planar IBL design shifts the guard rings on the ohmic side beneath the outer pixels. The length of these outer pixels is extended to 500 μm to keep the sensor width constant (see Fig. 2). A distortion on the electric field on the sensor edge will be introduced by this layout, but the charge collection after irradiation occurs primarily in the region directly beneath the n^+ implant.

The planar IBL sensors have been produced at CiS [8] (Germany) which also supplied ATLAS with sensors for the current Pixel Detector.

3.2. 3D sensors

In 3D pixel sensors the column-like electrodes penetrate the substrate, instead of being implanted on the wafer surface [9]. The depletion region thus grows parallel to the wafer surface. The ~10 μm diameter columns are alternatively n- and p-type doped defining the pixel configuration. The 3D design allows the reduction of the charge collection path without reducing the amount of sensor material the charge particles traverse.

IBL 3D sensors have been manufactured in two production facilities, CNM [10] (Spain) and FBK [11] (Italy), with the same