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ASIC developments for high speed serial data transmission in particle physics experiments

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ABSTRACT

We report R&D results on two integrated circuit designs: a 5 Gbps 16:1 serializer and a 5 GHz LC phase-locked-loop (PLL). The prototypes were fabricated with a commercial thin-film silicon-on-sapphire 0.25 μm CMOS technology. Both the serializer and the PLL have been evaluated to meet design goals and tested against operation conditions in the environment of a particle physics detector front-end for the proposed HL-LHC upgrade.

1. Introduction

Serial data transmission over optical fibers is used in particle physics experiments. The transmitting data rate over a single fiber channel increased from a few megabits per second (Mbps) to 1.6 gigabits per second (Gbps. Example: the optical link that reads out the Liquid Argon Calorimeter [1], or LAr, in the ATLAS experiment at CERN). The operation environments require high system reliability due to lack of frequent access for maintenance or repair. In some cases the radiation in a particle physics detector front-end also puts special requirements on the electronics and optics that operate inside the detector volume [2]. In the upgrade program for the High Luminosity Large Hadron Collider (HL-LHC) at CERN, R&D projects are carried out to meet the challenges of higher radiation tolerance and system reliability, and much higher data bandwidth with low power dissipation, compared with the optical link systems now operating in experiments on the LHC. This is because with the increase of radiation in the detector front-end, it is advantageous to simplify the front-end readout electronics by moving all level-1 triggering circuits to the back-end data acquisition (DAQ) system where frequent access is possible and there is no or very little radiation in the operation environment. The price to pay in the data-streaming mode front-end electronics is on the data transmission bandwidth. Taking the ATLAS LAr optical link as an example, the data throughput will increase from 1.6 Gbps per front-end board (FEB) to over 100 Gbps per FEB. To meet this challenge, and to address the needs in many new detectors' readout R&D, especially those designs to operate in radiation environment, we have been working on designs of Application Specific Integrated Circuits (ASICs) for the transmitting side of an optical link. The final goal of data throughput in our R&D program is 10 Gbps per fiber. As a step towards that goal, we prototyped a 16:1 serializer designed to operate at 5 Gbps, and an LC based phase-locked-loop (PLL) that runs up to 5 GHz. Both designs are based on a commercial thin-film silicon-on-sapphire (SOS) 0.25 μm CMOS technology. The design and measurement results of the serializer are reported in Section 2, while those for the LC-PLL in Section 3. In the conclusion we point out our roadmap to the final goal of ASICs and the link system of 10 Gbps per fiber, or an aggregated bandwidth of 120 Gbps per FEB.

2. Design and measurement results of the 5 Gbps serializer ASIC

A functional block diagram of serial data transmission over fiber optics is shown in Fig. 1. The interface block prepares the upstream parallel data for serial transmission hence works at a clock rate that is close to the parallel data clock which is much lower (by about 8 × in this case) than the serial data rate. The serializer and the optical interface blocks have circuits that work at the highest clock frequency of the system. For example, for a 5 Gbps serial data rate and circuits using both edges of the clock, one needs a 2.5 GHz PLL. The optical interface consists of a (current) laser driver (LD) circuit and a laser. The LD is the same as a CML line driver with matching modulation current and impedance of the laser in use. Because of these, we decided to first prototype a 16:1 serializer with a CML output to gain experience with this SOS technology. To increase the chances of success, this design is also based on a ring oscillator PLL as its clock unit, learned from a successful previous ASIC serializer, the

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GOL chip, developed for particle physics [3]. This PLL limits the serial speed to be 5 Gbps. To probe the speed of the technology, we also implemented a standalone LC based PLL. The design and testing of this serializer are described in the following subsections while the LC-PLL is described in Section 3.

2.1. The design of the ASIC

The design of the serializer follows an inverted tree structure with a cascade of many 2:1 multiplexing units, as shown in Fig. 2. The advantage of this serializing structure are twofold: one, the multiplexers operate at lower speeds except the last stage which runs at the final serial data rate, offering the possibility of "trading power for speed" only in the last multiplexer which is specially designed; two, the power-of-2 structure simplifies the design of the clock unit, which in this particular design is shared with the PLL divider chain. A divide-by-two divider immediately after the VCO (voltage controlled oscillator) in the PLL also helps to maximize the clock speed. The disadvantage of this structure is a serializing ratio of the power of 2, requiring a possible data reformatting at the interface stage in front of the serializer. Since in most applications such an interface ASIC will be needed to perform many functions such as data framing, scrambling, redundancy switch, and communication for control and monitoring, adding data bus reformatting to the interface to cope with a particular application is manageable. The high-speed clock is synthesized based a ring-oscillator-PLL, also illustrated in Fig. 2. The PLL can be selected to latch to either the rising or the falling edge of the reference clock (the parallel input data clock), ensuring correctly clocking in the input data. A selection of PLL low pass filter bandwidth is implemented to cope with different input clock quality. A static D-Flip–Flop is used to improve the serializer's immunity to single event upset caused by ionizing particles. To achieve the needed speed with these static DFF, its internal clock and clock-bar are carefully adjusted to ensure the shortest D-to-Q time.

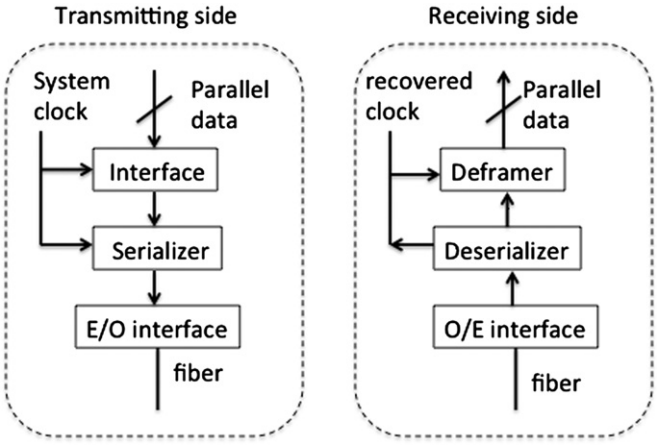

Fig. 1. Block diagram of a fiber optics based serial link system.

2.2. The evaluation of the prototype

Testing of the prototype chip was carried out by wire-bonding it to a PCB. Special caution was exercised for a few very fast signals both in the PCB design with impedance-matched traces and in placing the chip for wire-bonding with the shortest connecting wires. In general electric signal reflection is minimized by implementing impedance match for all differential signal traces. For CMOS signal traces, resistors are placed in series to reduce sharp rising (falling) edge. Shown in Fig. 3(a) is the eye diagram measurement with an eye mask. A bathtub curve is also traced with a Bit-Error-Rate-Tester (Anritsu MP1763C/1764C) and is shown in Fig. 3(b). From both measurements one can extract an eye opening of 0.69 UI (Unit Interval). Signal rise/fall time, amplitude of a 100 Ω differential load, timing jitter in the serial bit stream, together with different jitter components are listed in Table 1. The measured power consumption of this ASIC is 463 mW, corresponding to 93 mW/Gbps. This measured power consumption in room temperature agrees with simulation within 5%.

2.3. The next step in serializer design

Making use of the fact that in most particle physics detector front-end electronics, all readout channels are based on one system clock, we decided to design an array serializer, with two serializing units sharing one LC-PLL. The choice of this architecture is a balance of power saving and high-speed clock distribution. A block diagram of this design is shown in Fig. 4. The designed serial data rate is 8 Gbps, as shown in the post-layout simulation of the output eye diagram. The simulated power consumption of this ASIC is 1200 mW, or 75 mW/Gbps. This design reaches the highest achievable serial data rate with the particular process we choose in this SOS technology, with all the constraints we have, in particular the radiation tolerance requirement.

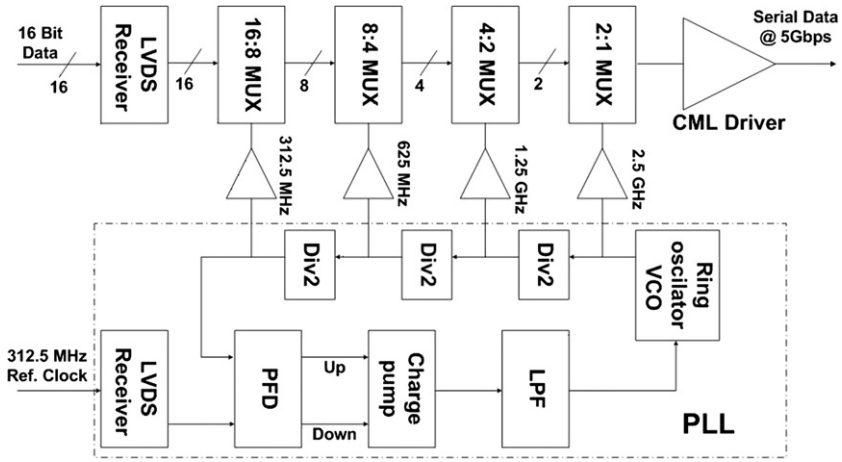

Fig. 2. Block diagram design of the 16:1 5 Gbps serializer.