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Exponential signal synthesis in digital pulse processing

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ABSTRACT

Digital pulse processing allows the synthesis of exponential signals that can be used in pulse shaping and baseline restoration. A recursive algorithm for the synthesis of high-pass filters is presented and discussed in view of its application as a baseline restorer. The high-pass filter can be arranged in a gated baseline restorer configuration similar to widely used analog implementations. Two techniques to synthesize time-invariant, finite impulse response (FIR) cusp shapers are presented. The first technique synthesizes a true cusp shape in the discrete-time domain. This algorithm may be sensitive to round-off errors and may require a large amount of computational resources. The second method for synthesis of cusp shapes is suitable for implementation using integer arithmetic, particularly in hardware. This algorithm uses linear interpolation to synthesize close approximations of true cusp shapes. The algorithm does not introduce round-off errors and has been tested in hardware.

1. Introduction

Exponential signals are essential for the formation of detector signals and pulse shaping in radiation measurements. Exponential signals can be found in noise analysis and optimal pulse shaping [1,2]. Historically RC–CR circuits have been used to shape detector pulses. The R–C low pass filter has an impulse response, which is a decaying exponential signal. The step response of the C–R high pass filter is also a decaying exponential signal. With the development of digital techniques to process detector pulses various pulse shape synthesis algorithms were introduced that resemble cusp shapes [3,4]. This paper describes efficient digital techniques to synthesize exponential signals including the true cusp shape. The algorithms and the system descriptions use discrete-time signal notations, basic signal definitions and graphical system blocks as defined in reference [5]. It should be noted that the functional block diagrams are graphical representations of digital signal processing operations and not of actual hardware blocks or software routines. These operations accept and generate a sequence of signal samples by performing instantaneous operations. Synchronous hardware designs will require accurate data synchronization, which can be achieved by accounting for any delays associated with the hardware-implemented arithmetic and logic operations.

2. Digital synthesis of exponential signals

Mathematically the exponential signals in the discrete time domain are defined by

$$y(n) = \begin{cases} a^n & \text{for } n \geq 0 \\ 0 & \text{elsewhere} \end{cases} \tag{1}$$

where a is called an exponential base [5]. In digital signal processing n is the index of the consecutive values (samples) of the discrete-time signal. If $a=0$ or $a=1$ then all samples $y(n)$ for $n \geq 0$ are constant (equal to 0 or 1, respectively). If the exponential base a is greater than 0 but less than 1, $y(n)$ is a decaying exponential signal. If a is greater than 1 then $y(n)$ is a growing exponential signal. If a is negative then $y(n)$ alternates between positive and negative numbers. In this paper we consider the exponential base a to be greater than zero.

From Eq. (1) the ratio of two consecutive values of an exponential signal can be expressed as

$$\frac{y(n)}{y(n-1)} = \frac{a^n}{a^{n-1}} = a \tag{2}$$

for $n > 0$ and $y(0)=1$.

Using Eq. (2), a growing or decaying exponential signal can be expressed in the following recursive form

$$y(n) = ay(n-1) \tag{3}$$

for every n, given the initial conditions $y(0)=1$ and $y(n)=0$ for $n < 0$.

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The goal of exponential signal synthesis is to define a linear time-invariant (LTI) recursive system that produces an exponential signal in response to an input signal $x(n)$. This system can be described using a first order difference equation [5]

$$y(n)=x(n)+ay(n-1) \quad (4)$$

The output signal $y(n)$ represents an exponential signal only when the conditions $y(0)=1$ and $y(n)=0$ for $n<0$ are fulfilled. These conditions are met when the system is relaxed [5] by forcing delayed term $y(n\text{-}1)=0$ for $n<0$, and when the input signal $x(n)$ is the unit impulse $\delta(n)$ ($x(n)=\delta(n)$). In this case the output of the system $y(n)$ is the system's infinity impulse response (IIR) $h(n)$

$$h(n)=\delta(n)+ah(n-1) \quad (5)$$

for $n\geq 0$ and $h(n)=0$ for $n<0$. It is clear that this impulse response is an exponential signal, which grows or decays infinitely in time.

The functional block diagram of a system with an exponential impulse response, as defined by Eq. (5), is illustrated in Fig. 1b. The recursive algorithm requires three functional blocks: an adder, a unit delay and a constant multiplayer. This system, when excited by a unit impulse $\delta(n)$, will generate exponential signals that are either growing (Fig. 1c) or decaying (Fig. 1d). The growth/decay rate is determined by the magnitude of the multiplication coefficient a which is the exponential base of the output exponential signal. The system depicted in Fig. 1b is a basic functional block for the synthesis of cusp shapers that will be discussed later in this paper.

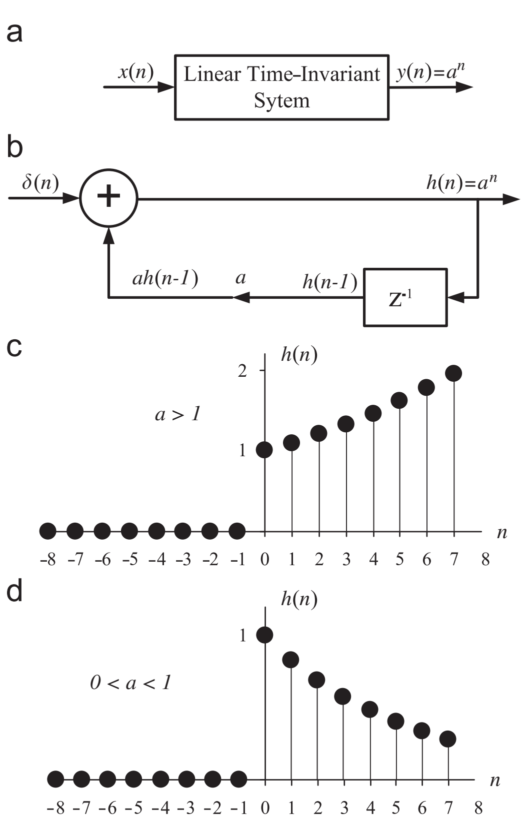

Fig. 1. Block diagrams: (a) of a system synthesizing exponential signals and (b) exponential unit impulse response. Examples are shown of: (c) a growing exponential impulse response and (d) a decaying exponential impulse response.

3. High-pass filter

High pass filters are used in pulse shaping as well as in baseline restorers of radiation spectrometers [2,6,7]. The C–R differentiation is widely used as a pulse conditioning circuit in spectroscopy amplifiers. In some cases pole-zero cancelation circuits are used to achieve a single real pole exponential response. The step response of a high-pass C–R filter is a decaying exponential signal with decay time constant equal to CR.

In the discrete-time domain a decaying exponential signal can be synthesized as a response to a unit step $u(n)$ ($x(n)=u(n)$). In Fig. 2a functional block diagram of such a system is shown. The system implements a recursive algorithm using a constant multiplier, an accumulator (ACC) and a subtractor. It is important that an initial condition of the system is established. Particularly, the accumulator needs to be reset to zero before any non-zero digital signal values are applied to the system input, e.g $w(n)=0$ for $n<0$.

At any time the accumulator output $w(n)$ contains the sum of all weighted output values preceding $y(n)$.

To derive the unit impulse response of the system the accumulator response is expressed as a function of the weighted output signal. The accumulator response is given by the sum of all previous $cy(i)$ values, and $w(n)$ is the same, shifted by a unit delay

$$w(n)=\sum_{i=-\infty}^{n-1} cy(i) \quad (6)$$

Let $x(n)=u(n)$ and $w(n)=0$ for $n<0$. These conditions define $y(n)=0$ for $n<0$. The unit step response of the system $y(n)$ is then given by the following equation:

$$y(n)=x(n)-w(n)=u(n)-\sum_{i=0}^{n-1} cy(i) \quad (7)$$

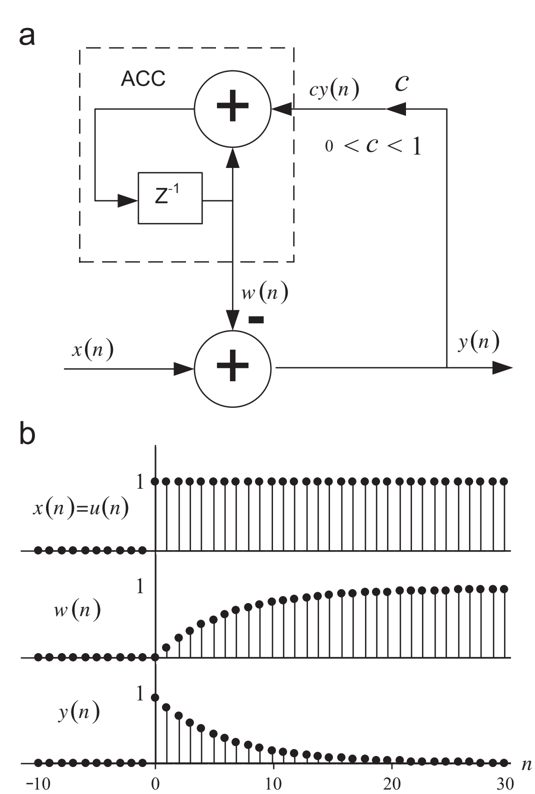

Fig. 2. A digital high-pass filter: (a) functional block diagram and (b) its response to a unit step signal.