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Characterisation of a pixel sensor in 0.20 μm SOI technology for charged particle tracking

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ABSTRACT

This paper presents the results of the characterisation of a pixel sensor manufactured in 0.2 μm SOI technology integrated on a high-resistivity substrate, and featuring several pixel cell layouts for charge collection optimisation. The sensor is tested with short IR laser pulses, X-rays and 200 GeV pions. We report results on charge collection, particle detection efficiency and single point resolution.

1. Introduction

Monolithic Si pixel sensors have become an established technology for precision vertex tracking in particle physics and in charged particle detection and photon imaging. Commercial bulk CMOS is the most commonly adopted process for monolithic active pixel sensors (MAPS) [1]. MAPS are being successfully applied to particle physics experiments [2,3], imaging in transmission electron microscopy [4–6] and photon imaging [7]. However, MAPS in bulk CMOS technology have several limitations. First, only nMOS or pMOS transistors can be built without disturbing the signal charge collection. Then, the charge collected from the thin epitaxial layer is small, limiting the achievable signal. The collection occurs through diffusion in an almost field-free region, which results in a long charge collection time (of order of 100 ns [8]) and increased sensitivity to radiation damage [9]. The silicon on insulator (SOI) technology makes it possible to fabricate CMOS circuits on a thin Si layer, insulated from the handle wafer by a buried oxide layer (BOX). A high-resistivity Si handle wafer provides a sensitive volume that can be biased, thus improving both the speed and the quantity of the charge carrier collection generated by an ionising particle. Vias through the BOX connect the substrate to the electronics layer, where both nMOS and pMOS transistors can be built.

The appealing features of the SOI technology for developing pixel detectors were recognised a decade ago in a pioneering study [10–12]. It has been with the availability of a commercial SOI process with small feature size CMOS from the collaboration between KEK, Tsukuba and OKI Semiconductor Co. Ltd that a systematic R&D effort on SOI pixel detectors has started [13,14]. The KEK-OKI Semiconductor process has special vias cut into the BOX to contact the underlying handle wafer and collect the charge signal. A technology proof of principle for charged particle tracking was obtained with the successful test of a prototype in 0.15 μm SOI technology on a particle beam [15]. Together with the detection of the first particles in the SOI pixels, one of the main challenges for the further development of the technology appeared. The bias applied to the high-resistivity substrate induces a potential below the CMOS electronics layer which is shielded only in part by the BOX. This potential acts as a backgate to the transistors shifting their thresholds. As a result of this "backgating" effect, the charge sensing and read-out electronics could only be operated for low to moderate depletion voltages V_d, up to 15–20 V [16], and thus the charge was collected by a depleted region of modest thickness, 25−50 μm depending on the handle wafer resistivity. In that prototype sensor a series of

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guard-rings was used to counter the back-gating effect. Guard-rings take considerable space in the pixel and are only partially effective. Instead, the implant of a buried p-well (BPW) beneath the BOX and the transistors has been found to successfully screen the potential applied to the high-resistivity layer in single transistor test structures [17,18]. This motivates the adoption of a BPW in the design of pixel cells immune from back-gating.

In this paper we present the characterisation of two pixel structures of a test chip fabricated in 0.2 μm SOI technology, which implements different pixel cells designed to minimise the back-gating effect.

2. Chip description

The prototype chip, named "SOImager-2", derives its global architecture from the earlier "SOImager-1" chip [19]. In order to optimise the design of the pixel cell for mitigating the back-gating effect and enhancing the charge collection, pixel cells of different design are implemented. The chip is manufactured by OKI Semiconductor Co. Ltd in 0.2 μm SOI technology on n-type SOI wafers with a nominal resistivity of the handle wafer of 700 Ω cm.

The sensitive area is a $3.5 \times 3.5\ mm^2$ matrix of 256×256 pixels arrayed on a 13.75 μm pitch. In order to increase the speed of the serial read-out, the pixel matrix is divided into four parallel arrays of 64 columns each. Each array is connected to four identical parallel output analog stages. Both the pixel cell and the ancillary electronics are designed and tested to operate at up to 50 MHz read-out frequency. The chip read-out implements a global shutter. Guard-rings are implemented around the pixel matrix (p+ I/O) and the peripheral I/O electronics (p+ Outer) in order to insulate the transistors from the effect of the potential below the BOX. The pixel cell keeps the same 3 T design of the earlier prototype for the whole matrix, but the pixel array is now divided into eight different 64×128 pixel sectors, each implementing a different layout. These layouts explore different diode sizes, configurations of floating and grounded guard-rings around the pixel, as well as the use of a buried p-well (BPW). In this paper we report results for two pixel cell designs with no p-type guard-ring and BPW connected to the pixel diode. One pixel cell (type I) has a 1.5 μm diode with a large BPW layer extending beneath the whole pixel. The second design (type II) features a larger diode (5 μm) with a BPW layer which extends below the diode only.

3. Chip tests

I–V and *C–V* characteristics are obtained in the laboratory to determine the evolution of the leakage current with the depletion voltage, the breakdown voltage and to estimate the thickness of the depleted region. The sensor is then tested in the laboratory with short IR laser pulses of various wavelengths and X-rays. The laser diode is driven by a fast voltage pulse applied through a bias-tee which feeds the laser with a constant current. A 2 ns-long laser pulse is generated, transported using a single-mode optical fibre and focused to a $\simeq 5$ μm spot on the pixel front surface. The detector is mounted on a remotely controlled precision stage, which allows us to vary its position with an accuracy of ≤ 1 μm. The laser pulse is triggered in phase with the detector data acquisition cycle and has an adjustable delay. Laser tests allow us to measure the charge carrier signal and collection time as a function of V_d. By varying the laser spot position along pixel rows and columns, the charge sharing on neighbouring pixels is also investigated. X-rays are used to calibrate the pixel and study the linearity of its response with deposited charge. We use 5.9 keV X-rays from a ^{55}Fe source and fluorescence radiation from Ti, Fe and Cu targets illuminated with a monochromatic 12 keV synchrotron radiation beam at the LBNL Advanced Light Source (ALS).

The response to energetic charged particles is studied with 200 GeV/c π^- on the H4 beam-line at the CERN SPS. Three SOImager-2 sensors have been arranged in a beam telescope configuration (see Fig. 1). The first two chips, spaced by 9.4 mm, are mechanically aligned and surveyed using a metrology machine before installation into a doublet unit. The third chip, located 36 mm downstream (called singlet in the following), is installed on a remotely controlled rotation stage. After installation on the beam-line, the three sensors have been aligned by optical survey. The final alignment is performed using particle tracks. Data is acquired at a rate of ~ 150 events s^{-1} during the 9.8 s-long SPS extraction spill. The detector temperature is kept stable at $(20 \pm 1)\ ^\circ C$ by flowing cold air inside the optical enclosure housing the detectors.

For the lab and beam tests, the chip is mounted on a mezzanine board, which carries four analog pre-amplifiers, each receiving the signal from one of the four chip analog outputs. Signals are routed into differential lines and fed to the data acquisition system through 1 m-long twisted pair cables with standard USB connectors. The data acquisition system consists of an analog board pigtailed to a commercial FPGA development board, used as control unit [20]. Both boards are powered by a stand-alone integrated power supply, which also supplies the detector bias. The analog board has five independent analog differential inputs, which have been used to read-out one analog output from each of the detectors in the doublet and two outputs of the singlet. Each differential input stage feeds a 100 MS/s 14-bit ADC. The control board has a Xilinx Virtex-5 FPGA which supplies the clocks and the slow control signals driving the sensor chips and routes the digitised data to a high speed FIFO to be formatted

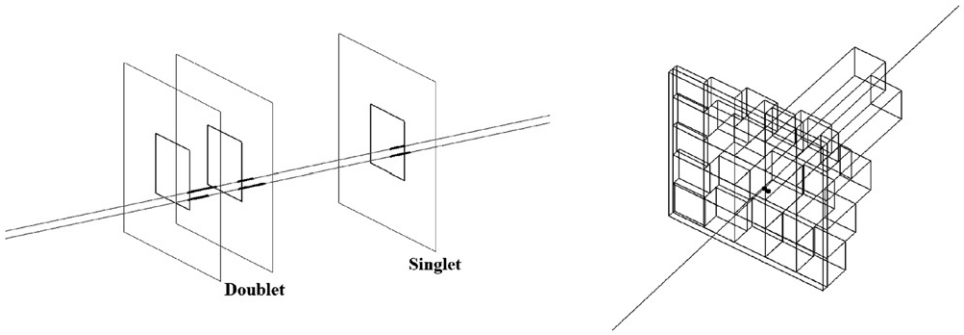

Fig. 1. (Left) Schematic layout of the SOI sensors for the SPS beam test. The first two planes on the left make up the detector doublet, the plane on the right, called singlet, was mounted on a remotely controlled rotation stage. Two pion tracks reconstructed in a single event are shown. (Right) Individual pixel response in a cluster on the second doublet plane associated to an extrapolated track.