



## Online calibration and performance of the ATLAS Pixel Detector

Markus Keil <sup>a,b,\*</sup>

<sup>a</sup> CERN, 1211 Geneva 23, Switzerland

<sup>b</sup> II. Physikalisches Institut, Universität Göttingen, Friedrich-Hund-Platz 1, 37077 Göttingen, Germany

### ARTICLE INFO

Available online 10 December 2010

Keywords:

LHC

Pixel detectors

Tracking detectors

### ABSTRACT

The ATLAS Pixel Detector is the innermost detector of the ATLAS experiment at the Large Hadron Collider at CERN. It consists of 1744 silicon sensors equipped with approximately 80 million electronic channels, providing typically three measurement points with high resolution for particles emerging from the beam-interaction region, thus allowing measuring particle tracks and secondary vertices with very high precision. The readout system of the Pixel Detector is based on a bi-directional optical data transmission system between the detector and the data acquisition system with an individual link for each of the 1744 modules. Signal conversion components are located on both ends, approximately 80 m apart.

This paper describes the tuning and calibration of the optical links and the detector modules, including measurements of threshold, noise, charge measurement, timing performance and the sensor leakage current.

© 2010 Elsevier B.V. All rights reserved.

### 1. Introduction

The ATLAS Pixel Detector [1,2], shown in Fig. 1, is the innermost tracking detector of the ATLAS experiment [2]. It is made of three concentric barrel layers with mean radii of 50.5, 88.5 and 122.5 mm centred around the beam axis and two endcaps with three discs each, forming a three-hit system up to pseudo-rapidities of  $\pm 2.5$ . The full detector contains 1744 pixel modules, which are mounted on carbon fibre local supports. An evaporative  $C_3F_8$  cooling system is incorporated into the local supports to absorb the heat produced by the modules and to allow for an operation at temperatures below 0 °C, to limit the effects of radiation damage.

The individual pixel modules (Fig. 2) are made of a 250  $\mu\text{m}$  thick n-on-n silicon sensor, 16 front-end chips and a module controller chip (MCC) [3]. The sensor is divided into 47,232 pixels with a typical pixel size of 50  $\mu\text{m}$   $\times$  400  $\mu\text{m}$ ; approximately 10% of pixels have a size of 50  $\mu\text{m}$   $\times$  600  $\mu\text{m}$  (long pixels) to bridge the gaps between the readout chips in the long pixel direction. Another 2.5% of the electronics channels have two sensor pixel connected to bridge the gaps in the other direction (ganged pixels). The sensor is read out by 16 front-end chips with 2880 electronics channels each. Each pixel cell contains a charge sensitive preamplifier, a discriminator and the necessary digital readout logic to transfer hits to the peripheral circuitry of the chip, the end-of-column (EOC) logic. In the EOC logic hits are stored up to the programmable trigger latency and sent to the module controller chip in case a trigger

arrives at the correct latency, and erased otherwise. Together with the mere hit location and time, the time-over-threshold (ToT) information is read out for each hit. This is the time interval during which the preamplifier output is above the threshold, in units of the bunch crossing clock (25 ns). Due to the pulse shape of the preamplifier the ToT is a nearly linear function of the deposited charge. Evaluating this ToT information can therefore be used to infer the charge deposited by a passing particle. The routing of signals and power lines of the module is done on the flex hybrid. This is a flexible polyimide PCB, which is glued onto the backplane of the sensor. The connection to the front-end chip is made with wire bonds. The flex hybrid also carries the MCC, which controls the front-end chips and performs an event building with the hit data received from the front-end chips. The off-module connection is provided by a micro-cable, which is either soldered directly onto the flex hybrid (in case of the disc modules) or connected to a polyimide pigtail (in case of the barrel module). Fig. 2 shows the elements of a pixel barrel module.

The transmission of fast signals (data, clock and commands) between the detector and the readout crates in the counting rooms is achieved via optical links. One TTC link per module (Timing, Trigger and Commands) carries the clock and commands to the detector, a data link brings the hit data from the detector to the readout crates. Most modules have one associated data link, only the modules in the innermost barrel layer have two data links per module to accommodate the higher data rate. The electro-optical conversion on the detector side is done on optoboards, which are located at a distance of approximately 1 m from the interaction point. Fig. 3 shows the overall readout scheme of the ATLAS Pixel Detector, from the sensor to the off-detector electronics in the counting room.

\* Correspondence address: CERN, 1211 Geneva 23, Switzerland.

E-mail address: [markus.keil@cern.ch](mailto:markus.keil@cern.ch)

<sup>1</sup> On behalf of the ATLAS Collaboration.

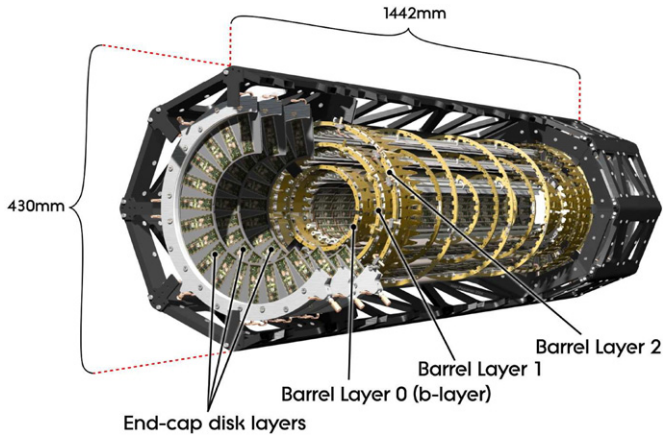


Fig. 1. Schematical drawing of the ATLAS Pixel Detector. The detector comprises three barrel layers and two endcaps with three discs each. The individual detector modules are mounted on carbon fibre support structures with incorporated cooling circuits.

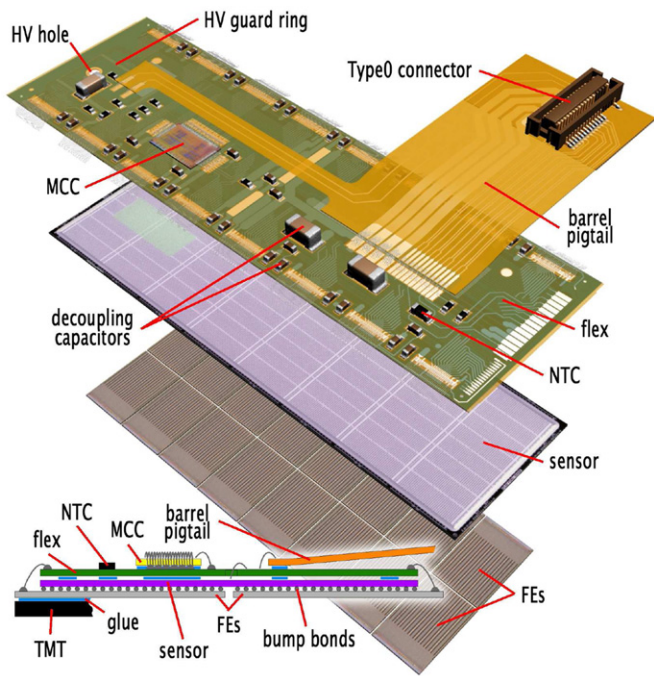


Fig. 2. Assembly view and cross-section of an ATLAS Pixel Detector module. Sixteen front-end chips are bump bonded to the silicon pixel sensor. Interconnections are done on a flexible polyimide PCB, which is connected by wire bonds to the electronics chips.

## 2. Calibration measurements

### 2.1. Tuning of the optical links

In order to establish the communication between the detector modules and the off-detector electronics in the counting room, the optical links need to be tuned [4]. The most critical parameters are the threshold and the sampling phase of the uplink, which sends the hit data from the module to the readout crates. The correct settings of these parameters for each module are determined in the so-called BOC scan. This scan performs a bit error rate measurement, scanning the full two-dimensional parameter space of delay and threshold. A typical scan result is shown in Fig. 4. White areas indicate no errors, all remaining regions have non-zero error rates. One sees an error floor for low thresholds, indicating noise which is interpreted as logical one, due to a too low threshold setting. The vertical error band corresponds to a sampling at a moment when the data transmitted is not stable but changes from one clock cycle to the next. An optimal operating point is chosen within the error free regions, taking into account also possible fluctuations of the different error regions.

In case of need the laser power of the on-detector lasers can be adjusted. However the modularity for this adjustment is 6 or 7 modules, depending on the exact location of the modules. For the inner layers and the discs a similar tuning is performed at a readout speed of 80 MBit/s. Currently all tunable modules (i.e. modules without more serious problems of the optical links) have been tuned without problems.

### 2.2. Threshold and noise

The electronics parameters of the front-end pixel cells are assessed by means of a programmable charge injection circuit in the front-end chip. The timing and the amount of charge can be freely chosen, allowing to perform all necessary tunings and a wide range of measurements. To measure the threshold and noise values, injections are performed with charges around the expected threshold and for each charge the number of hits for a fixed number of injections are counted. The values of threshold and noise are then extracted from an error function fit to the obtained response curve [5].

In order to set the thresholds as homogeneously as possible, a similar scan is performed; however for this so-called threshold tuning the injected charge is fixed to the target threshold value and in each pixel the setting of the tune-DAC, which determines the discriminator threshold, is varied. The setting for which the response fraction is as close as possible to 50%, is the ideal setting for the given target threshold [5].

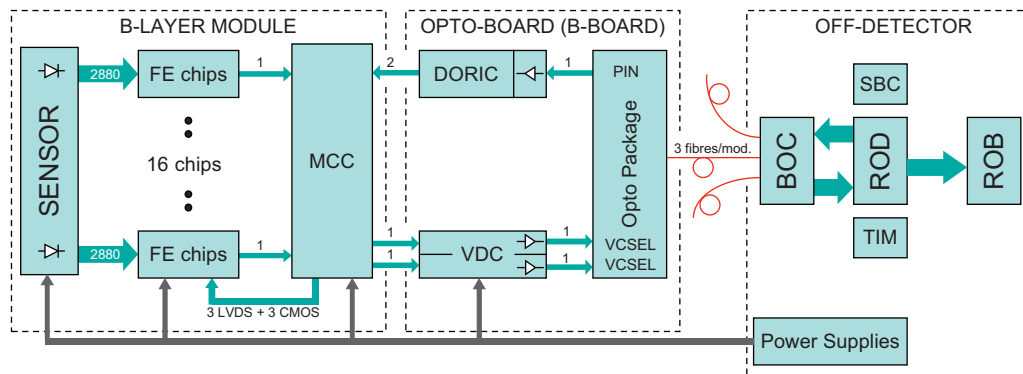


Fig. 3. Block diagram of the ATLAS Pixel Detector readout system architecture.

Download English Version:

<https://daneshyari.com/en/article/1824709>

Download Persian Version:

<https://daneshyari.com/article/1824709>

[Daneshyari.com](https://daneshyari.com)