Nuclear Instruments and Methods in Physics Research A 650 (2011) 79–83

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

EIGER: Next generation single photon counting detector for X-ray applications

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ARTICLE INFO

Available online 15 December 2010

Keywords:
Synchrotron radiation instrumentation
Photon counting
Pixel detectors
CMOS electronics

ABSTRACT

EIGER is an advanced family of single photon counting hybrid pixel detectors, primarily aimed at diffraction experiments at synchrotrons. Optimization of maximal functionality and minimal pixel size (using a 0.25 μm process and conserving the radiation tolerant design) has resulted in 75×75 μm^2 pixels. Every pixel comprises a preamplifier, shaper, discriminator (with a 6 bit DAC for threshold trimming), a configurable 4/8/12 bit counter with double buffering, as well as readout, control and test circuitry. A novel feature of this chip is its double buffered counter, meaning a next frame can be acquired while the previous one is being readout. An array of 256×256 pixels fits on a $\sim 2 \times 2$ cm^2 chip and a sensor of $\sim 8 \times 4$ cm^2 will be equipped with eight readout chips to form a *module* containing 0.5 Mpixel. Several modules can then be tiled to form larger area detectors. Detectors up to 4×8 modules (16 Mpixel) are planned. To achieve frame rates of up to 24 kHz the readout architecture is highly parallel, and the chip readout happens in parallel on 32 readout lines with a 100 MHz Double Data Rate clock.

Several chips and *singles* (i.e. a single chip bump-bonded to a single chip silicon sensor) were tested both with a lab X-ray source and at Swiss Light Source (SLS) beamlines. These tests demonstrate the full functionality of the chip and provide a first assessment of its performance. High resolution X-ray images and "high speed movies" were produced, even without threshold trimming, at the target system frame rates (up to $\sim$24 kHz in 4 bit mode). In parallel, dedicated hardware, firmware and software had to be developed to comply with the enormous data rate the chip is capable of delivering. Details of the chip design and tests will be given, as well as highlights of both test and final readout systems.

1. Introduction

The success achieved by the PSI-SLS detector group with the development of Pilatus [1] and Mythen [2] encouraged the research for a much more advanced family of pixel detectors. Careful analysis of the state of the art (e.g. [1,3–5]) before starting the design phase (late 2004) and discussions with PSI beamline scientists highlighted several features which were considered crucial. These were either not available at all, or not all available in the same system.

For this reason EIGER, a new hybrid pixel detector with smaller pixels, faster frame rate and negligible dead time, is being developed by the PSI-SLS detector group to supersede the previous generation of PILATUS detectors. High radiation tolerance, and in particular large area coverage, typical of PILATUS detectors, are two main assets of EIGER detectors.

EIGER is primarily aimed at diffraction experiments at synchrotron light sources. Typical applications [6–8] include Protein Crystallography, Small Angle X-ray Scattering (SAXS), Coherent Diffraction Imaging, X-ray Photon Correlation Spectroscopy, Scanning SAXS and Surface Diffraction.

2. EIGER readout chip

2.1. Readout chip main features

Table 1 summarizes the main specifications and features of the EIGER Readout chip (ROC). UMC 0.25 μm technology was chosen because of its high quality and reasonable price. The drawback of this choice is that Hardening By Design (HBD) layout techniques [9,10] had to be used to achieve the required high radiation tolerance (>4 Mrad). The chip size (19.3×20 mm^2) was chosen to be as close as possible to the maximum reticle size of the technology. Some basic digital cells were designed with extremely compact HBD layouts to estimate the maximum achievable transistor density. A first estimate of the pixel area (based on the required pixel functionality) was then calculated, resulting in an array of 256×256 pixels of 75×75 μm^2.

The chip design features several advances with respect to state of the art hybrid pixel detectors. Double buffering (i.e. a new frame can be acquired while the previous one is readout), extremely short dead time (less than 3 μs) and a frame rate up to $\sim$24 kHz (in 4 bit

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doi:10.1016/j.nima.2010.12.005

Table 1
Summary of the main specs and features of the readout chip.

Readout chip specifications and features	
Technology	UMC 0.25 μm
Power supplies	1.1 V (ana.), 2 V (dig.), 1.8 V (I/O)
Radiation tolerance	Rad-tolerant design (>4 Mrad)
Pixel array	$256 \times 256 = 65\,536$
Chip size	19.3×20 mm^2
Frame rate	Up to ~ 24 kHz (in 4 bit mode)
Dead time	<3 μs
Pixel size	75×75 μm^2
Transistor count	430/pixel
Pixel counter	Configurable (4, 8, 12 bit mode), binary, double buffered for continuous readout
Threshold adjust	6 bit DAC/pixel
Other features	Overflow control, single pixel addressing and analog out for testing

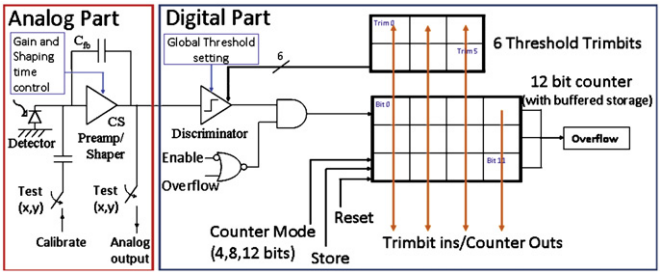

Fig. 1. Schematic representation of the pixel architecture.

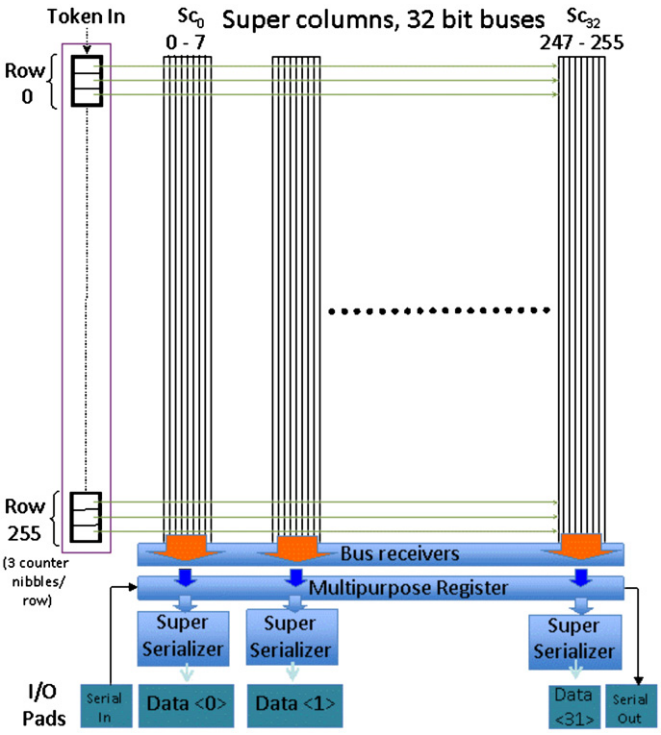

Fig. 2. Schematic representation of the EIGER readout architecture.

mode) are implemented in a single HBD pixel. Furthermore, due to the high modularity and parallelism embedded both in the chip and in the readout system, this is also the corresponding maximum nominal detector frame rate, irrespective of the detector size.

2.2. Pixel architecture

The pixel electronics, schematically represented in Fig. 1, implement a single photon counting architecture.

The charge signal from the sensor is amplified and filtered by a low noise preamplifier and following shaper with tunable shaping time and gain. The shaped signal is fed to a comparator which has a threshold voltage given by a global reference voltage (Vcmp) plus an on-pixel trim DAC (6 bit). An incoming signal exceeding this threshold toggles the comparator state. If the chip is in *Expose* mode and the pixel counter did not overflow, the comparator pulse increments the following digital counter by one. At the end of the exposure time the counter content is temporarily stored in a pixel buffer and the counter is reset to allow a new exposure to start immediately.

During the *Readout* phase the state of the pixel buffers is transferred to the chip periphery for readout (see Section 2.3). Because neither test structures nor small scale prototypes were designed, special care was taken in designing the chip testability. For example, every pixel can be individually addressed for testing and preliminary calibration prior to bump-bonding to a sensor. When the chip is in *Test* mode the calibration circuitry of the selected pixel injects a known charge into the pixel input and tracks the shaper output of the chosen channel so that it can be monitored with an oscilloscope. Precise calibration with a monochromatic X-ray source is performed after bump-bonding to a sensor.

2.3. Readout architecture

Fig. 2 shows a schematic diagram of the chip readout scheme. The readout architecture is optimized for very fast frame rates. Therefore a high level of parallelism is embedded in the chip. A *side shift register* (SSR, 256×3 cells long) is fed with a token at the beginning of the readout phase (TokenIn). The token travels through the SSR with a frequency of 6.25 MHz, selecting a full row of pixel counter nibbles (4×256 bits). These 1024 counter bits are transferred in parallel to the periphery readout logic. The high number of signal busses active at the same moment, which moreover have to cross the whole chip, can generate a high level of digital to analog crosstalk, that could severely affect the performance of the pixel's analog sections. To mitigate this effect the bit content is not sent to the periphery as a CMOS signal, but as a current step of ~ 10 μA. This current is then converted to a voltage level by a bank of 1024 current comparators placed at the receiving end of the signal busses and latched to a Multi-Purpose Register (MPR) that in *Image acquisition* mode works just like a buffer (parallel in/parallel out).

In the chip periphery columns are grouped together in blocks of eight to form independent *supercolumns*. The counter bits of a supercolumn (4×8, stored in the MPR) are serialized with a faster clock (100 MHz Double Data Rate, DDR) by dedicated circuitry (*superserializer* in Fig. 2). The readout of the resulting 32 supercolumns, each served by one superseliarizer, happens in parallel on 32 outputs.

To set all the on-pixel trim DAC bits the chip is set to *Program* mode. In this case the MPR is reconfigured as a serial shift register with parallel out, where the trim bits for a full row are transferred serially through a dedicated input (SerialIn). Once the register is full the bits are transferred to the target pixel row in parallel via the same set of internal signal busses used for data readout.

To increase chip testability a fully serial readout mode of operation is also implemented. In this case the pixel readout happens in the standard way down to the MPR, but there the data is not superserialized and read out on the 32 parallel data lines, but fully serialized on a single dedicated line (SerialOut).

In *Readout test* mode the MPR can be preloaded with a specific pattern via SerialIn, and be read out by the superserializers. This