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Characterisation of "n-in-p" pixel sensors for high radiation environments

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ABSTRACT

This work presents the first held at Liverpool University measurements of pixel sensors with n-type readout implant in the p-type bulk before and after irradiation of samples by 24 GeV protons to doses 7×10^{15} and 1.5×10^{16} protons/cm^2. A comparison is given for two measurement techniques; one based on the FE-I3 readout chip designed for the ATLAS and the other using the Beetle chip developed for the LHCb experiments at CERN.

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1. Introduction

In the future luminosity upgrade of the Large Hadron Collider at CERN pixel sensors are anticipated to occupy a larger volume to satisfy the need of increased granularity imposed by the much higher track density. The total surface covered by pixel sensors would go from present ~1.8 to 10 m^2 in the upgraded ATLAS detector. This significant increase in area can justify the use of cost-effective p-type silicon bulk instead of present n-type for the n-type readout pixels needed for enhanced radiation tolerance. Savings up to 50% come from avoiding double-sided photolithography required for the back-plane of n-type silicon to implant a diode structure there.

The much larger area short strip detectors have already adopted such an approach as a default with 10×10 cm^2 detectors now being delivered. It has been proven that "n-in-p" (n-type readout implant in the p-type bulk) segmented silicon sensors offer radiation tolerance similar to the "n-in-n" ones, fully satisfying the requirements for all pixel layers of the upgraded experiments. On the other hand, the bias voltage required to operate heavily irradiated sensors has to be remarkably high (up to 1000 V for the innermost layers). It must be demonstrated that "n-in-p" silicon pixel detectors can be biased to this level without electrical breakdown or discharges through the overlapping readout chip.

Novel technologies resulting from research and development programmes (R&D) on radiation-tolerant detectors need planning for being transferred to large scale applications for optimisation of performance and expenses. Pixellated detector assemblies (where the electronics is hybridised by bump-bonding to the sensors themselves) are particularly valuable due to high production costs. At the system level, engineering of the front-end services, i.e. power feed, cooling, etc. should provide reliable operation of sensors throughout their lifetime. Having long traditions in design and construction of the silicon tracking detectors [1,2], the Oliver Lodge Laboratory of the Liverpool University can contribute substantially to the ATLAS upgrade.

The "n-in-p" planar technology is being evaluated at Liverpool University as a candidate for the future strip and pixel detectors. It has already been shown [3] that after expected dose of 2×10^{16} neq/cm^2 they still produce signals compatible with 99% efficient tracking. Variety of vendors, low manufacturing costs (the DC-coupled pixel sensors require 3 or 4 mask levels only) and high production yield are evident advantages of the "n-in-p" process in the entire class of semiconductor particle detectors. The paper describes the development programme of planar pixel sensors at Liverpool University in collaboration with the Micron Semiconductor Ltd.[1]

2. Pixel sensor design

Studies of pixel detectors at Liverpool University have started with the preparation of a new wafer containing devices reproducing the geometry of standard ATLAS pixel sensors [4] for a single chip assembly (SCA) based on the FE-I3 chip [5]. The SCA detector with its 2800 pixels has been redesigned to be read out by only two Beetle chips [6]. The new sensor has eight interleaved pixels per column connected to one wire bond pad at the die boundary, Fig. 1. Such a geometry allows for the cluster size measurements up to 7 pixels with 50 μm pitch. In the second version of that detector every other pixel (400 μm long) in the row is connected to the same wire bond pad. The readout pixel matrix consists of 128×16 implants grouped for the column-parallel (APC) or row-parallel (APR) readout. The second metal was needed for the pixel interconnect.

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Fig. 1. Sensor with interleaved readout pixels. Second metal layer provides their interconnect and routing to the wire bond pad. Shuffling of readout channels minimises their cross-talk.

A possibility of wire bonding at room temperature is one major advantage of these detectors for irradiation and annealing studies. Re-use of their bonding pads makes it possible to irradiate them without the readout chip. Furthermore these devices facilitate measurements of the punch-through voltage, inter-strip resistance and capacitance before and after irradiation.

APC and APR devices were manufactured in 2009 by Micron Semiconductor Ltd. on 300 μm thin 6-in. wafer in the double-metal "n-in-p" process on float-zone silicon with 13 kOhm cm bulk resistivity and the p-spray isolation [7]. The wafer includes also strip detectors with bias options and pads for testing the high voltage performance of guard structures and dicing schemes. In addition the RD50 collaboration[2] has provided prototypes of the ATLAS pixel sensors (produced by Micron Semiconductor Ltd. on float-zone p-type silicon with 10 kOhm cm bulk resistivity) which were used for populating the SCAs.

3. Characterisation of sensor layout components

A detailed analysis was needed to characterise the new detector structures including the matrix of readout implants, high voltage termination (multiple floating guard rings) and dicing options. Their influence on the readout electronics (before and after irradiation), their operating limits and tolerance to layout variations were investigated.

Prior to measurements all sensors underwent several HV cycles to the breakdown point with the current limitation at 1 μA. Most of detectors could stand the maximum voltage of Keithley 2410 source-measure unit of 1100 V. For some other devices the HV training (burn-in) has helped to improve the breakdown voltage by almost 30% up to 900 V after which the IV and CV characteristics of pixel sensors were obtained to check that the reverse bias voltage could be applied safely for the full bulk depletion. However, the HV performance of SCA detectors had degraded (probably due to excessive thermal and mechanical stress) after their bump bonding at the Fraunhofer Institute.[3]

The silicon sensors, the SCAs and some test structures were irradiated by protons at IRRAD-1 facility [8] at CERN to doses 7×10^{15} and 1.5×10^{16} protons/cm^2.

3.1. Measurements of readout implants

Each pixel features a punch-through biasing circuit that connects the readout implant to the bias grid through a narrow gap of an accumulation layer. The build-up voltage between the grid and readout implants, called "punch-through voltage" U_{pt}, was measured using a Keithley 6517A electrometer for gap lengths ranging from $L=3$ to 50 μm. The voltage across the gap for unirradiated sensor follows one-to-one the reverse bias voltage applied either to pixels or to the grid. For the APC irradiated to 7×10^{15} protons/cm^2 this dependence is about 50 times weaker. After reaching the value $U_{pt}\approx 1$ V/μm $\times L$ (μm) the punch-through voltage becomes independent of further increase of the bias voltage for both measurement samples. The readout electronics connected to the pixel sensor has to cope with this voltage. To comply with absolute maximum ratings of deep-submicron CMOS process the potential of the bias grid bump bonded to the FE-I3 chip on the SCA was controlled to be equal to an average potential of pixels. For measurements with the Beetle chip the bias grid of the APC was left floating.

Isolation of pixels from the bias grid (gap resistance) was parameterised as an inverse slope of the IV characteristics with the voltage differential (smaller than U_{pt}) applied between the readout implants and the grid. The number of joined pixels was increased to eliminate the systematic error and for all pixels in parallel their gap resistance at room temperature and before irradiation was in the TOhm range, independent of the bias voltage above 50 V. For the APC irradiated to 7×10^{15} protons/cm^2 the gap resistance of all pixels in parallel at -25 °C was 100 kOhm, independent of the bias voltage above 1 kV. Similarly, the inter-strip resistance was measured between two groups of implants (even and odd columns of the APC). It equals to 200 GOhm/cm for the non-irradiated sensor at room temperature with the bias voltage above 50 V and 10 MOhm/cm at -25 °C and 1 kV bias for the APC irradiated to 7×10^{15} protons/cm^2.

The IV and CV scans were made for the entire pixel matrix through its bias grid. The full depletion voltage amounts to 80 V for unirradiated APC detectors as found from the $1/C^2$ plot. However this technique cannot be used for irradiated sensors and therefore one relies on the charge collection measurements. The reverse leakage current density at 600 V amounts to 25 nA/cm^2 for the unirradiated APC detector at room temperature and 60 and 100 μA/cm^2 for doses 7×10^{15} and 1.5×10^{16} protons/cm^2 at -25 °C. The breakdown voltage of all APC samples exceeds 1100 V.

3.2. Studies of the guard structures

The breakdown voltage of a bare implant with 600 μm distance to the cut edge is about 150 V before irradiation that is well above the full depletion voltage of 80 V. However, the ratio between the full depletion and breakdown voltages becomes worse for irradiated implant in this geometry. The optimum HV range could be significantly extended by using guard rings. Several diodes with different guard structures: varying gaps

[2] http://rd50.web.cern.ch

[3] Fraunhofer IZM Gustav-Meyer-Allee 25, D-13355 Berlin, Germany.

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