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# The neon gas field ion source—a first characterization of neon nanomachining properties

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ABSTRACT

At the Charged Particle Optics Conference (CPO7) in 2006, a novel trimer based helium gas field ion source (GFIS) was introduced for use in a new helium ion microscope (HIM), demonstrating the novel source performance attributes and unique imaging applications of the HIM (Hill et al., 2008 [1]; Livengood et al., 2008 [2]). Since that time there have been numerous enhancements to the HIM source and platform demonstrating resolution scaling into the sub 0.5 nm regime (Scipioni et al., 2009 [3]; Pickard et al., 2010 [4]). At this Charged Particle Optics Conference (CPO8) we will be introducing a neon version of the trimer-GFIS co-developed by Carl Zeiss SMT and Intel Corporation. The neon source was developed as a possible supplement to the gallium liquid metal ion source (LMIS) used today in most focused ion beam (FIB) systems (Abramo et al., 1994 [5]; Young et al.,1998 [6]). The neon GFIS source has low energy spread ($\sim$1 eV) and a small virtual source size (sub-nanometer), similar to that of the helium GFIS. However neon does differ from the helium GFIS in two significant ways: neon ions have high sputtering yields (e.g. 1 Si atom per incident ion at 20 keV); and have relatively shallow implant depth (e.g. 46 nm in silicon at 20 keV). Both of these are limiting factors for helium in many nanomachining applications. In this paper we will present both simulation and experimental results of the neon GFIS used for imaging and nanomachining applications.



## 1. Introduction–background

Focused ion beam (FIB) silicon machining is used today for analysis and circuit modification of semiconductor devices. Applications include TEM sample preparation and cross-sectioning for analyzing defects and performing CD metrology measurements [5,6]. One of the most challenging FIB applications is silicon backside circuit modification. For this application transistor devices and interconnects are accessed through the backside of the silicon substrate on flip-chip mounted packaged die.

Fig. 1 shows an example of a complex circuit modification performed through the silicon backside of a microprocessor, where several signals (metal interconnect wires) were rerouted to modify the circuitry to enable a timing modification of the circuitry [7]. For this application, high aspect ratio vias must be nano-machined through a few microns of remaining silicon to access the transistors and interconnect wires buried below. The size of these vias must scale with every process generation in order to allow access to the desired transistors without damaging other adjacent transistors and device signals. In other words, this must be done as non-invasively to the microprocessor as possible.

One of the key challenges of performing silicon nanomachining is scaling the technology and capability to keep up with the scaling tread-mill of semiconductor process technology. Semiconductor processes follow "Moore's Law", which states that transistor density will double every two years, thus the transistor minimum dimensions must scale by 50%. Correspondingly, nanomachining capabilities must also scale at the same rate. Fig. 2 shows cross-sections of FIB-vias demonstrating the geometry scaling requirements over an 8 year period. In that time frame, FIB-vias cross-sectional area has decreased by $\sim 100\times$, and is expected to shrink by an additional $4\times$ by 2013—when the 14 nm process technology node ramps into production. If nanomachining is to continue to provide circuit modification and analysis capabilities on devices, FIB probe sizes must scale beyond the 7 nm FWHM size available in commercial CE tools today.

## 2. Neon GFIS source

In exploring alternative FIB ion source technologies, the trimer-GFIS source developed by Ward et al. [1,2,8] for the helium

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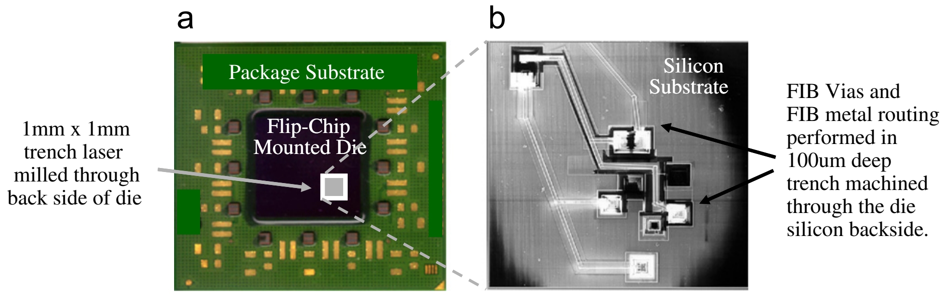


**Fig. 1.** Example of a circuit edit performed through the silicon backside of a flip-chip mounted microprocessor. (a) is a global view of the flip-chip die mounted on the C4 package and (b) is a zoomed in view of the circuit edit performed at the base of the large access hole laser machined in the silicon substrate.

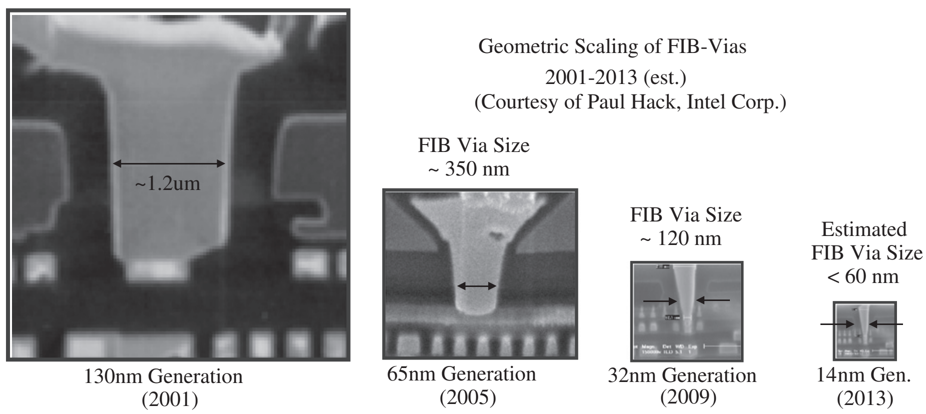


**Fig. 2.** Cross-section of FIB-vias, demonstrating minimum FIB-via geometry requirements for a 12 year period.

ion microscope (HIM) looked to be very promising based on its inherently small probe size ( $<$ 0.5 nm) and high resolution imaging capabilities ( $<$ 0.3 nm). Both of these are critical attributes for circuit edit of shrinking geometries. And indeed, some very impressive results for nano-fabrication have been demonstrated using the HIM by Delft-Technical University and TNO, as well as others. Recent publications by Alkemade et al. [9], have demonstrated sub 10 nm nano-wires depositions and sub 10 nm cuts in thin Au membranes. However, in studies conducted by Tan et al. on the characterization the HIM for circuit edit applications, the conclusion was that the helium implantation depth in silicon (400 nm at 30 keV) was not compatible with the tight nanomachining circuit edit geometries. Further, it was concluded that the helium ion beam's low sputter yields were insufficient for the complex material removal requirements of circuit edit applications [10].

After the conclusion of the helium analysis, we began exploring alternative noble gasses, such as neon, argon, and xenon, which might be compatible with the GFIS source technology. One of the key attributes required for a stable GFIS source is to have a noble gas with an ionization energy that is higher than other gas contaminants that could be present in the source region. The table in Fig. 3a shows the ionization energies for several noble gases as well as various impurities. Helium and neon are the only two noble gasses that possess sufficiently high ionization energies relative to impurities that might otherwise contaminate the source region. Thus when the ion source is operated optimally for neon or helium, any impurities in the source region will ionize prior to reaching the trimer tip region. More details of the neon source development and emission stability characteristics are discussed by Notte et al. [11].

## 3. Experimental results

The neon GFIS beam characterization was done on an engineering test platform at Carl Zeiss, SMT research and development labs in Peabody, MA. The base engineering platform consisted of: (1) GFIS ion source configured for neon operation, (2) an electrostatic optical column designed for neon ion species, (3) Orion$^{TM}$ microscope base vacuum system, stage, and related scan and imaging electronics.

The experiments focused on characterizing the source stability, emission properties, probe size, image resolution, and the beam material interaction properties. The material interaction experiments were done for three different materials commonly used in semiconductor devices: copper, silicon, and a silicon-oxide. Tests were performed over a range of beam energies, beam currents, and ion doses.

Beam energy range: 10–30 kV
Beam current range: 200 fA–2 pA
Ion dose range: 1E+16–1E+18 ion cm$^{-2}$

### 3.1. Resolution and probe size analysis

Edge resolution tests were performed on a HOPG (highly oriented Pyrolytic graphite) sample, which has sharp features ideal for image analysis. High resolution images were captured with 1 pA beam current and beam energies of 10, 25, and 28 kV. The images were analyzed using various resolution analysis algorithms to measure the edge transition width. The resolution results shown in Fig. 4 are the average values taken from three different measurement algorithms. The best resolution achieved for the neon beam was 1.3 nm (average)