Nuclear Instruments and Methods in Physics Research A 636 (2011) S237–S241

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Performance study of SOI monolithic pixel detectors for X-ray application

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ARTICLE INFO

Available online 5 May 2010

Keywords:
SOI
Pixel detector
CMOS
X-ray detector

ABSTRACT

We are now developing Silicon-on-insulator (SOI) monolithic pixel detectors for X-ray and charged particle applications in collaboration with OKI Semiconductor Co., Ltd. The detector development project started in 2005 and the SOI process for pixel detectors was developed. We developed some prototypes of SOI pixel detectors. Specifically, integration type and counting type pixel detectors were irradiated with a continuous red laser, infrared laser and X-rays and their performances were studied. One of the issues in the SOI detectors is the back-gate effect, that is, higher back bias voltages affect the characteristics of SOI-CMOS transistors. As a result of the new process step to protect the device against the back-gate effect, images with higher back bias voltages were obtained in the integration-type pixel detector. We also confirmed the dependence on 8 keV X-ray intensity for the counting type pixel detector. In 2009, new versions of the detectors were designed to improve their performances with X-rays and charged particles.

1. Introduction

Silicon-on-insulator (SOI) technology refers to the utilization of a layered silicon–insulator–silicon substrate. A SOI-CMOS circuit is formed on the top layer called SOI layer and has lower power consumption and lower parasitic capacitance compared with a conventional silicon (bulk CMOS) circuit. SOI-based devices have been used in microelectronics industry such as CPUs and processors used in TV games, etc. Since two types of silicons with different resistivities are available in a SOI wafer, high resistivity silicon can be used as a sensor and low resistivity silicon as an electric circuit. In this case, a truly monolithic image detector can be achieved.

The Detector Technology Project (DTP) at KEK was started in 2005. We started a feasibility study of monolithic pixel detector using SOI technology. The LSI process on SOI wafer is based on 0.2 μm CMOS fully depleted-(FD-) SOI process in OKI Semiconductor Co., Ltd [1]. We have operated a Multi Project Wafer (MPW) run every year since 2007 in which universities and laboratories around the world share the process cost and the numerous designs are put together. The SOI monolithic detector is feasible for various applications such as high-energy physics experiment, X-ray spectroscopy, space industry, medical use and so on. When the SOI detector is used for X-ray applications, the good points are the following: (i) the detector directly detects X-rays up to about 20 keV, (ii) good position resolution below a few tens of μm with high detection efficiency can be achieved, (iii) bump or wire bonding to sensors is not required and therefore material can be minimized, and (iv) the X-ray detector with high-speed and low-power consumption readout system can be achieved because parasitic devices capacitance is lower. In order to achieve good X-ray sensitivity, the SOI monolithic detector requires a few hundreds of volts on the back side. However, a week point of the SOI detector is the "back-gate effect" [2]—higher back bias voltages cause the potential to increase just below the SOI transistors and therefore the properties of the transistors change. Due to this phenomenon, enough voltage could not be applied. In 2009, a new process has been applied to protect the device for the back-gate effect. In this report, the performance and response to lasers and X-rays of the SOI detector are shown and the effects to the new process to the detectors are reported.

2. Pixel detectors

In the MPW run in 2007 (FY07), two types of pixel detectors were developed [3]. One is the integration-type pixel, called INTPIX2 and another is counting-type pixel, called CNTPIX2. In the MPW run in 2008 (FY08), updated version of the above pixels, called INTPIX3 and CNTPIX3, respectively, were developed. In this report, test results of INTPIX2, INTPIX3 and CNTPIX2 are shown and the design concept of CNTPIX3 is described.

In INTPIX2 and 3, the circuit is the standard 3 transistor CMOS active pixel sensor (3 T CMOS APS) with a storage capacitor [3,4].

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doi:10.1016/j.nima.2010.04.117

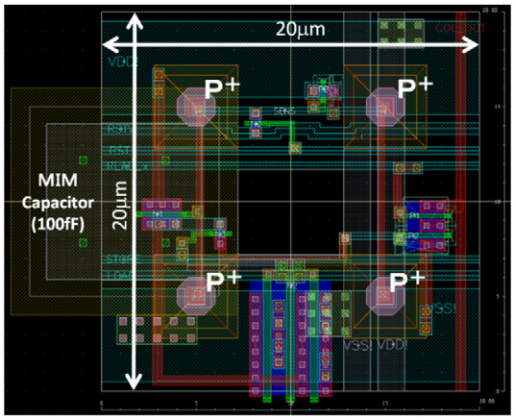

Fig. 1. INTPIX2 pixel layout.

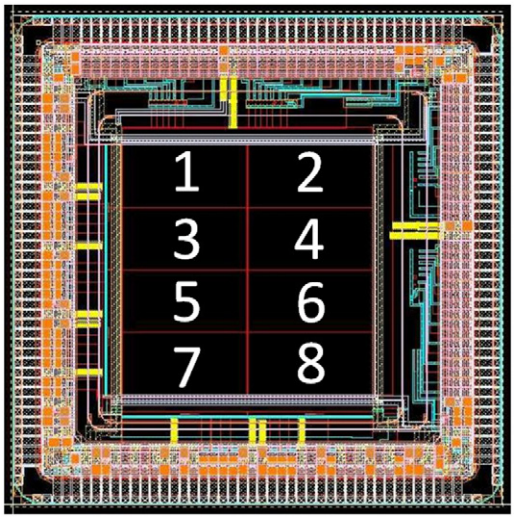

Fig. 2. Top layout of INTPIX3. No. 1–8 represents pixel type as shown in Table 1.

Table 1
Explanation of 8 types of pixel layout. Regions 1–3 include one p+ implant surrounded by BPW ring. The voltage of the ring can be controlled from the outside. The BPW in region 8 covers four p+ implants but does not cover the transistors.

Region	Explanation
1	2 BPW rings and 1p+ with BPW
2	A BPW ring and 1p+ with BPW
3	A BPW ring and 1p+ without BPW
4	4p+ without BPW (the same as INTPIX2)
5–6	4p+ with BPW
7	1p+ with BPW
8	4p+ with BPW (no BPW on transistor)

Fig. 1 shows the pixel layout of INTPIX2. There are four p+ implants to gain high charge collection efficiency. In INTPIX2 and 3, the pixel size is 20 μm × 20 μm, the number of pixels is 128 × 128 and the chip size is 5 mm × 5 mm. Signals are sent to column buffers followed by an analog output buffer circuit. INTPIX3 includes 8 kinds of pixel layouts. Each pixel group includes 64 × 32 pixels. Fig. 2 shows top layout of INTPIX3 and the explanation on 8 pixel types is shown in Table 1. The pixel layout in region 4 is the same as INTPIX2. The other regions are different and include a new process, buried p-well (BPW). Fig. 3 shows the pixel layout of region 6. The BPW is formed at the top of bulk

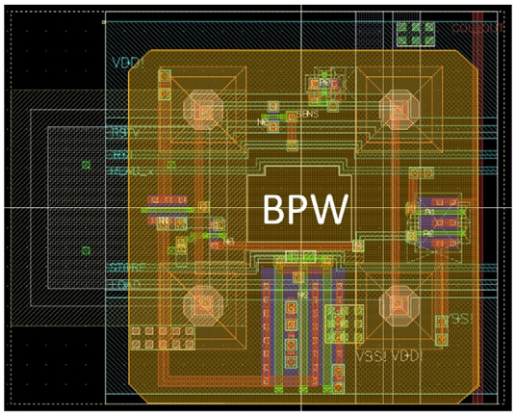

Fig. 3. Pixel layout of region 6. Orange shadow represents BPW. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article).

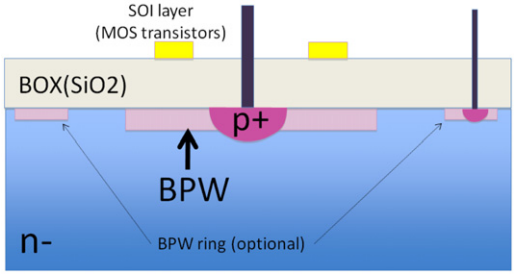

Fig. 4. Schematic diagram of SOI structure with BPW (side view).

silicon without removing materials in the SOI and SiO_2 layers as shown in Fig. 4. All peripheral circuits and I/O buffers are also covered by the BPW layer where the potential is adjusted from outside.

In CNTPIX2, each pixel circuit includes an amplifier, a dual discriminator and a 16 bit counter. Pixel size is 60 μm × 60 μm, the number of pixels is 128 × 128 and the chip size is 10.2 mm × 10.2 mm.

The detectors were mounted on a sub-board of SOI evaluation board with SiTCP [5] (SEABAS). The SEABAS equips two FPGA's and one controls the SOI logic and another handles the TCP/IP protocol. Output data from the SOI chip is sent to a PC via Ethernet cable. In INTPIX2 and 3, analog signal output is fed into a 65 MHz 12 bit ADC on the SEABAS.

3. Performance study

Integration-type and counting-type pixel detectors were irradiated with a continuous red laser, infrared (IR) laser and X-rays. The red laser is the Premier Laser Diode Module with 635 nm wavelength. IR laser is PicoQuant Pulsed Diode Laser (PDL) 800-B with 980 nm laser heads. A Rigaku FR-D Cu rotating anode generator (Rigaku Corporation) was used for X-ray irradiation. CuKα (8 keV) X-ray is dominant in FR-D and the cathode was running with tube voltages of 20–40 kV and tube currents of 5–40 mA. X-ray beam intensity was measured by Si PIN photodiode (Hamamatsu S3584-05) for calibration.

3.1. INTPIX2&3 test results

INTPIX2 and INTPIX3 were irradiated by IR laser (where the minimum pulse width is 50 ps (FWHM) and the maximum