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Readout ASICs for silicon drift detectors

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ABSTRACT

Semiconductor drift detectors (SDDs) are widely used in X-ray spectroscopy due to their excellent performances in terms of energy resolution and detection-rate. Suitable low noise readout electronics have to be designed in order to exploit the SDD intrinsic performances. The integration of this electronics in custom application specific integrated circuits (ASICs) is mandatory when the compactness of the detection system (detector and electronics) and the need to read out multi-elements SDDs are primary requirements. This work describes the development of three circuits for SDDs, which are a charge sensitive preamplifier operating in the pulsed reset regime, a fast shaping amplifier for high-count rates applications and a multi-channel ASIC that provides the whole analog processing and multiplexing of the signals from SDD arrays. The ASICs have been tested with SDDs with on-chip JFET and the results are presented here.

1. Introduction

Semiconductor Drift detectors (SDDs) have nowadays reached a leading position as detectors for X-ray spectroscopy due to their outstanding performances in terms of energy resolution and detection-rate [1,2]. The SDD's good performances are the result of their very small output capacitance. The integration of the input JFET of the preamplifier directly on the detector maximizes the benefits of the low anode capacitance. The SDD performances can nevertheless be exploited at best only with dedicated, and carefully designed, readout electronics. We present in this work few integrated circuits designed specifically for SDDs with integrated JFET. Integrated readout electronics is suitable either for SDDs with a small number of units (e.g. 1–4) when mounting and packaging require a very compact detection module, and for SDD arrays of several units (e.g. 100 units).

This work reports more specifically on the development of three circuits: a charge sensitive preamplifier operating in the pulsed reset regime, a fast shaping amplifier for high-count rate applications and a multi-channel ASIC with the whole analog processing and multiplexing of the signals for the SDD arrays. The experimental results obtained with these chips and with SDDs, provided by PNSensor GmbH (Munich, Germany), are also presented in the work.

2. A CMOS charge preamplifier with pulsed reset

The charge preamplifier operating in the pulse-reset regime is presently the most used solution, thanks to its low noise performances achievable at also at high counting rates [3]. The pulsed reset solution avoids the noise associated with the anode discharge current, which, in case of a continuous reset mechanism, would add its own noise contribution. The schematic principle of our implementation of the charge preamplifier is shown in Fig. 1. It consists of a conventional capacitive feedback configuration where the JFET (integrated on the SDD) is AC coupled to the remaining part of the preamplifier. The solution allows an independent biasing of the detector (including the JFET) and of the preamplifier. This is particularly useful for the independent choice of bias voltages and of the switch-on sequences of both detector and preamplifier. If the time constant $C_{in}R_{fb}$ is made sufficiently high, the circuit amplifies the signal with an open-loop voltage gain from the SDD anode to the preamplifier output given by $gm_{FET}R_{fb}$, where gm_{FET} is the transconductance of the JFET. The circuit presented in this work uses two external components for C_{in} and R_{fb}; however, a version of the preamplifier with integrated C_{in} and R_{fb} has been also produced [4]. The feedback capacitance of the preamplifier $C_{a\text{-}ig}$ consists of a parasitic capacitance between the inner guard

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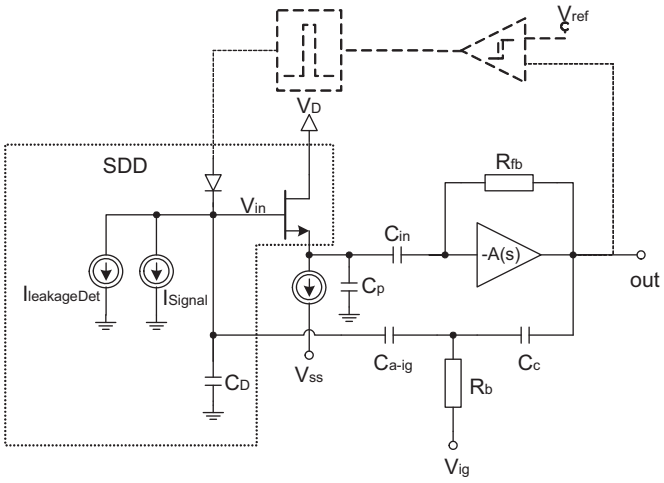

Fig. 1. The charge preamplifier configuration with pulsed reset mechanism.

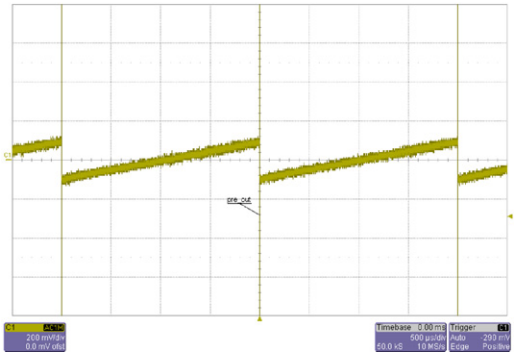

Fig. 2. Ramp at the output of one channel of the preamplifier ASIC in corresponding to the integration of the leakage current between two consecutive reset pulses.

ring, which separates the SDD anode from the JFET region, and the anode itself. Its value ranges from 20 fF for the droplet-type SDD [2] to 30 fF in the circular SDD. The preamplifier output is AC coupled to this capacitance, by means of C_c, also external to the chip, in order to allow the DC bias of the inner guard ring through R_b.

The preamplifier operation involves the integration of the detector leakage current on the feedback capacitance as well. This produces a voltage ramp at the output of the preamplifier, as shown in Fig. 2, in a measurement on the prototype developed here. When the output ramp exceeds a given value, a trigger circuit is activated, as schematically shown in Fig. 1, in order to provide a reset pulse on a diode integrated close to the SDD anode. The preamplifier can also operate with an external periodical pulsed reset regime.

A four channel version of the preamplifier has been realized (in the AMS 0.35 μm CMOS technology) and successfully tested. The circuit implements four channels of the type described in Fig. 1. The triggers fired by the output ramp are generated on the chip and their outputs are fed into a logic OR. When a channel fires the trigger, a common reset pulse is given all SDDs connected to the ASIC.

In Fig. 3, the charge preamplifier response corresponding to a signal produced by pulsing the first ring of the SDD is reported. The measured rise time of about 30 ns; is limited by the preamplifier itself; the drift/collection properties of the charge inside the SDD would cause a further increase in the rise time.

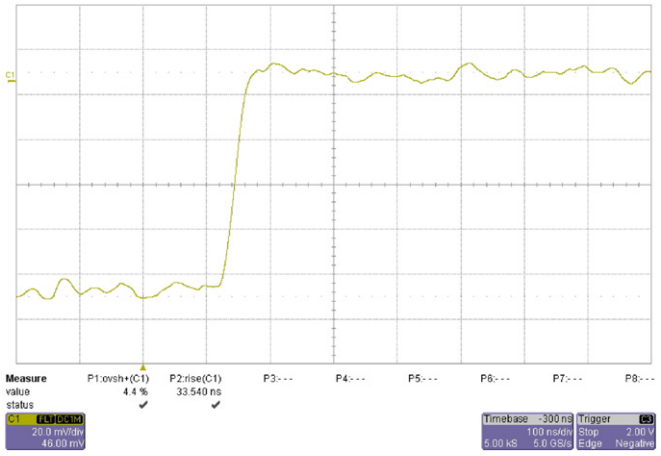

Fig. 3. Rise time of the charge preamplifier corresponding to an output signal produced by pulsing the first ring of the SDD. The measured rise time, of about 30 ns, is therefore limited by the preamplifier itself and not by the drift/collection properties of the charge inside the SDD.

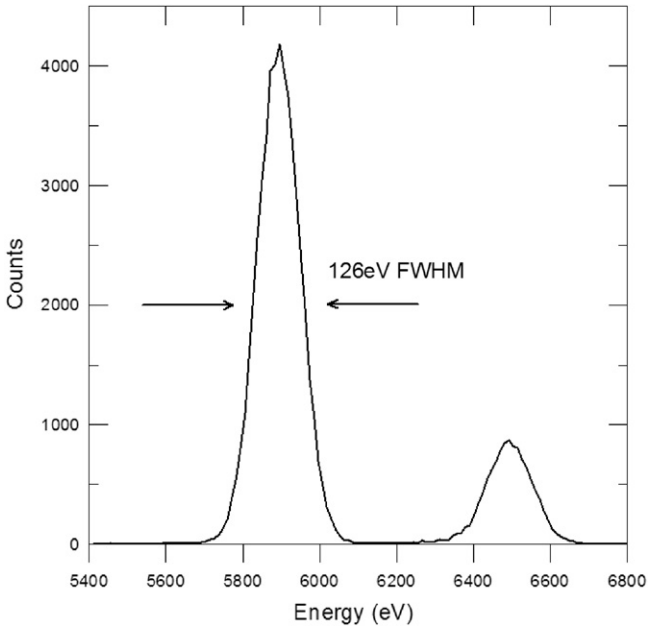

Fig. 4. Energy spectrum of a Fe-55 source measured with a droplet SDD of 10 mm^2 and the preamplifier ASIC. The shaping time is of 1 μs.

We tested the preamplifier in a spectroscopy measurement using a droplet SDD of 10 mm^2 cooled to −20 °C. The typical spectrum of a Fe-55 source is shown in Fig. 4. An energy resolution of 126 eV FWHM at the 5.9 keV line has been achieved with this preamplifier at 1 μs shaping time, similar to the one achievable with a hybrid version of the preamplifier. The energy resolution at 0.25 μs shaping time is of 139 eV FWHM. We have also tested the circuit at different counting rates. The energy resolution worsens to 128 eV at about 90.000 counts/s with a peak shift of about 0.2%.

3. An integrated fast shaping amplifier

We have developed a fully integrated high-order shaping amplifier, specifically designed for high counting rate measurements. It consists of a ninth order filter, optimized to achieve good electronics noise together with a reduced pulse width in order to