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# Introducing 65 nm CMOS technology in low-noise read-out of semiconductor detectors

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ABSTRACT

The large scale of integration provided by CMOS processes with minimum feature size in the 100 nm range, makes them very attractive in the design of front-end electronics for highly pixelated detectors, where several functions need to be packed inside a relatively small silicon area. Nowadays, processes with 130 nm minimum channel length are widely available for Application Specific Integrated Circuits (ASICs) design, nonetheless designers are considering more scaled technologies following the trend of commercial silicon foundries. This work provides an extensive analysis of the noise performance which can be attained by detector front-end circuits in a 65 nm CMOS process. The behavior of the 1/*f* and white noise terms in this technology node is studied as a function of the device polarity, of the gate length and width and of the bias conditions. A comparison with data from previous CMOS generations is also carried out to evaluate the impact of scaling down to the 65 nm node.

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## 1. Introduction

Deep-submicron CMOS commercial technologies have been extensively used for the development of front-end electronics in various High Energy Physics (HEP) detector applications. The distinctive features of these technologies have been exploited in particular in tracking systems where channel density and chip compactness together with a carefully optimized design for minimum noise, minimum power and radiation hardness are essential [1–3]. The specifications of vertex detectors at the next generation colliders (e.g., SLHC, ILC, Super B-Factory) ask for highly pixelated detectors with a small pitch (less than 20 μm in the case of ILC), with analog (amplification, filtering, discrimination and possibly even analog-to-digital conversion) and digital (data sparsification, time stamping and buffering) functions integrated in the pixel itself. These requirements apply both to the front-end electronics for hybrid pixels and to Monolithic Active Pixel Sensors (MAPS), where the readout electronics is built in the same substrate as the sensing electrodes. In order to comply with such requirements and to keep pace with the rapid evolution of CMOS technologies, readout integrated circuits for future particle tracking systems will be realized through fabrication processes with minimum feature size in the 100 nm range. The 130 nm CMOS generation is currently the focus of IC designers for the project of Application Specific Integrated Circuits (ASICs) in LHC upgrades and other detector applications, nonetheless designers are considering more scaled technologies following the trend of commercial silicon foundries [4–6]. In technologies beyond the 100 nm frontier peculiar features are used to match specifications of sub-100 nm CMOS nodes. These features include silicon strain in the channel region to increase charge carrier mobility [7,8] and the addition of nitrogen ("nitridation") to the gate oxide to increase its thickness and avoid an excessively large current leaking through the gate itself [9]. Moreover, the power supply voltage is not scaled as fast as silicon dioxide, allowing for an adequate dynamic range in analog applications. Beside these benefits, these process tricks might show some drawbacks. In particular it is not well known how they can affect critical aspects concerning the analog behavior of MOS devices such as noise performance and radiation hardness. In this work the behavior of the 1/*f* and white noise terms in a 65 nm CMOS process is studied as a function of the device polarity, of the gate length and width and of the drain current. A comparison is also carried out with data from previous CMOS generations to evaluate the impact of scaling down to the 65 nm node.

## 2. Experimental details

### 2.1. Investigated devices

The MOSFETs studied in this work belong to a 65 nm CMOS process manufactured by a commercial vendor which we will call

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Foundry A. Several variants of the 65 nm process technology exist in order to cover the whole foundry application space with various power and performance requirement. Device offering is classified as High Speed (HS), General Purpose (G) and Low Power (LP). In this work we characterized LP devices with standard threshold voltage (SVT). This variant concerns integrated circuits for which the leakage current must remain as low as possible, a criterion that ranks first in applications such as embedded devices, mobile phones or personal organizers. For this technology variant, the maximum allowed supply voltage $V_{DD}$ is 1.2 V for standard core devices which are the main focus of this work. We characterized PMOS and NMOS devices with gate lengths $L$ from 65 to 700 nm and widths $W$ from 20 to 1000 μm. The devices were laid out using a standard open structure, interdigitated configuration. For comparison purposes experimental data and measurements gathered from previous CMOS generations will be shown in the paper. In particular we will take into consideration data coming from a 90 nm CMOS process manufactured by the same foundry as the 65 nm process (Foundry A) and data coming from a 90 nm and a 130 nm CMOS processes provided by a second vendor which we will call Foundry B.

### 2.2. Measurement setup

Measurements of static and signal parameters were carried out by means of an Agilent E5270B Precision Measurement Mainframe with E5281B SMU Modules. The spectral density of the noise in the channel current was measured using instrumentation purposely developed at the Electronic Instrumentation Laboratory, University of Pavia. The noise of the DUT is amplified by a wideband interface circuit and detected by a Network/Spectrum Analyzer HP4195A [10]. This system allows for noise measurements in the 100 Hz–100 MHz range.

## 3. Experimental results

### 3.1. Device operating region

A key parameter for the signal and noise performance of a CMOS device is the transconductance $g_m$, whose behavior depends on the inversion region where the device is operating. The actual inversion level of a MOS transistor working in saturation can be expressed by means of its transconductance efficiency which is defined as the ratio of the transconductance $g_m$ to the drain current $I_D$. Fig. 1 shows a plot of the transconductance efficiency versus normalized drain current obtained for a PMOS and an NMOS belonging to the investigated 65 nm process.

The slope of the transconductance efficiency is zero in the weak inversion region, where the transconductance is proportional to the drain current, while, in strong inversion, the slope of $g_m/I_D$ on a log scale is $-\frac{1}{2}$, because the transconductance is proportional to the square root of the drain current. Moderate inversion is the transition region between weak and strong inversion. It is possible to define a characteristic normalized drain current $I_Z^*$ located at the intersection of the weak and strong inversion asymptotes, which can be assumed to be the center of the moderate inversion region [11,12]:

$$I_Z^* = 2\mu C_{OX} n V_T^2 \tag{1}$$

where $\mu$ is the channel mobility, $n$ is a coefficient proportional to the inverse of the subthreshold slope of $I_D$ as a function of $V_{GS}$ and $V_T = k_B T/q$ is the thermal voltage. According to Eq. (1) $I_Z^*$ is expected to be larger in NMOS and in devices fabricated in processes with smaller minimum feature size due to the larger value of $C_{OX}$. Therefore, the weak and moderate inversion regions extend to higher normalized drain currents in the most advanced CMOS generations. Fig. 1 shows that under reasonable power dissipation constraints, in the 65 nm node the preamplifier input device operates in the weak inversion region. For comparison purposes, values of $I_Z^*$ obtained for all the processes taken into account in this work have been gathered in Table 1. In all the examined processes, $I_Z^*$ was experimentally found to be independent of the device geometry. As expected $I_Z^*$ is always larger in NMOS with respect to PMOS due to the larger carrier mobility. In agreement with Eq. (1), technologies provided by Foundry B show larger values of $I_Z^*$ for the more scaled technology due to the larger $C_{OX}$. This behavior is not fulfilled for devices belonging to the two technology nodes provided by Foundry A. The lower value of $I_Z^*$ obtained for the 65 nm process with respect to the 90 nm process can be ascribed to unknown process details.

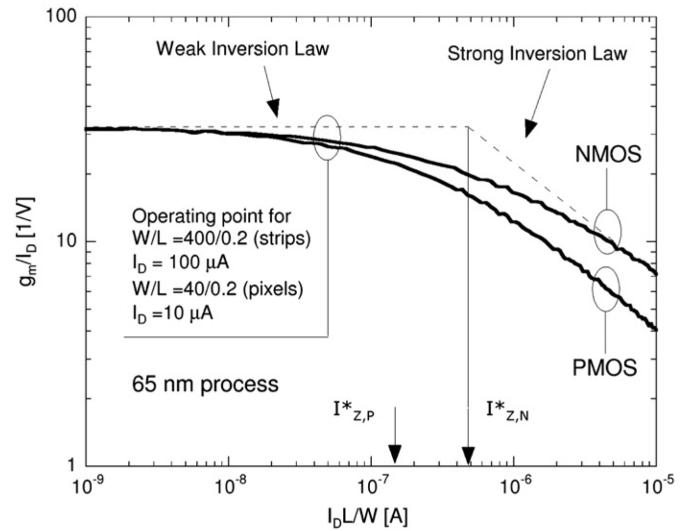


**Fig. 1.** Transconductance efficiency as a function of the normalized drain current for an NMOS and a PMOS in the 65 nm process with $W/L$=200/0.70. The measurement was performed at a drain-to-source voltage $|V_{DS}|$ = 1.2 V. The theoretical behavior of transconductance efficiency in weak and strong inversion region is also shown with a dashed line.

**Table 1**
Characteristic normalized drain current $I_Z^*$ [μA].

| | Foundry A | | Foundry B | |
|---|---|---|---|---|
| | 65 nm | 90 nm | 90 nm | 130 nm |
| NMOS | 0.49 | 0.74 | 0.75 | 0.55 |
| PMOS | 0.15 | 0.17 | 0.20 | 0.15 |

### 3.2. Gate leakage current

One of the constraining limits in the use of nanoscale technologies is the reduction of the gate oxide thickness into the direct tunneling regime. The gate current, being caused by discrete charges randomly crossing a potential barrier, results in an increase of the static power consumption for digital circuits and might degrade noise performance in analog applications, because of the shot and 1/$f$ noise contributions associated to $I_G$ [13]. Since the gate tunneling current strongly depends on the process recipe for the gate stack, gate current characterization is an appropriate tool to investigate the impact of nanoscale CMOS processing on the quality of the gate dielectric. While process

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