Nuclear Instruments and Methods in Physics Research A 624 (2010) 379–386

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Vertically integrated deep N-well CMOS MAPS with sparsification and time stamping capabilities for thin charged particle trackers ☆

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ARTICLE INFO

Available online 27 May 2010

Keywords:
DNW MAPS
CMOS
Vertical integration
Sparse readout
Low noise front-end electronics

ABSTRACT

A fine pitch, deep N-well CMOS monolithic active pixel sensor (DNW CMOS MAPS) with sparsified readout architecture and time stamping capabilities has been designed in a vertical integration (3D) technology. In this process, two 130 nm CMOS wafers are face-to-face bonded by means of thermo-compression techniques ensuring both the mechanical stability of the structure and the electrical interconnection between circuits belonging to different layers. This 3D design represents the evolution of a DNW monolithic sensor already fabricated in a planar 130 nm CMOS technology in view of applications to the vertex detector of the International Linear Collider (ILC). The paper is devoted to discussing the main design features and expected performance of the 3D DNW MAPS. Besides describing the front-end circuits and the general architecture of the detector, the work also provides some results from calculations and Monte Carlo device simulations comparing the old 2D solution with the new 3D one and illustrating the attainable detection efficiency improvements.

1. Introduction

Deep N-well CMOS monolithic active pixel sensors (DNW CMOS MAPS) were proposed a few years ago as possible candidates for charged particle tracking applications. They were specifically developed with the aim of enabling fast readout of large detector matrices through sparsification techniques [1]. In DNW-MAPS, the collecting electrode consists of a deep N-well integrating also NMOS devices from the analog front-end (AFE) section in the internal P-well. The collected charge is read out by a classical optimum chain for capacitive detectors, including a fully CMOS charge preamplifier which makes the charge sensitivity independent of the detector capacitance. Also CMOS digital blocks for sparsified data readout and time stamping are laid out in the elementary pixel cell. Based on the proposed device, the first ever MAPS detectors with pixel level sparsification have been fabricated and successfully tested at the Proton Synchrotron facility at CERN [2–4]. New technology options have been considered recently, in particular with the aim of improving such DNW MAPS properties as spatial resolution and detection and charge collection efficiency. Among the investigated technologies, vertical integration (also known as 3D) processes [5] seem the most promising ones. By stacking two or more standard CMOS layers (or tiers) one on top of the other, 3D processes may be very effective in providing, at affordable costs, increased functional density, physical separation of the analog front-end from the digital blocks and reduction of the area covered by competitive N-wells in the sensor layer. This paper describes the main design features and discusses the expected performance of a vertically integrated DNW CMOS MAPS detector, the SDR1 (sparsified digital readout) chip, specifically aimed at vertexing applications to the International Linear Collider (ILC) facility. The chip was designed in the framework of the 3DIC Consortium, a collaboration among Fermilab and French and Italian institutions pursuing the development and fabrication of vertically integrated front-end circuits and monolithic detectors. The SDR1 MAPS sensor represents the evolution of another monolithic detector, the SDR0 chip, previously designed and fabricated in a planar, 130 nm CMOS technology [2], to which reference will be made throughout this work for the sake of comparison. The paper is structured as follows. After this introduction, Section 2 will be concerned with a short description of the two-tier vertical integration technology used for the design of the 3D DNW MAPS. Section 3 will describe the detector architecture, providing some details on the pixel level analog and logic processors and on the digital back-end. Circuit simulation results will be also discussed in the same section. Finally, Section 4 will present some data from calculations and Monte Carlo device simulations emphasizing the achievable detection efficiency improvements through a comparison between the SDR0 and the SDR1 chip performance.

☆This work was supported by the Italian Ministry of University and Research through a National FIRB Project, contract #RBAP06L4S5.

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doi:10.1016/j.nima.2010.05.039

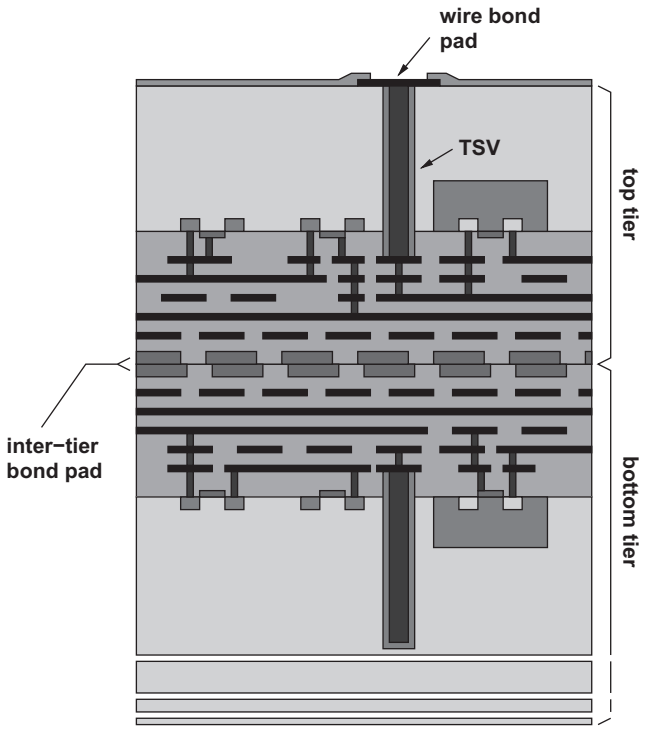

Fig. 1. Cross-sectional view of a double-layer 3D process.

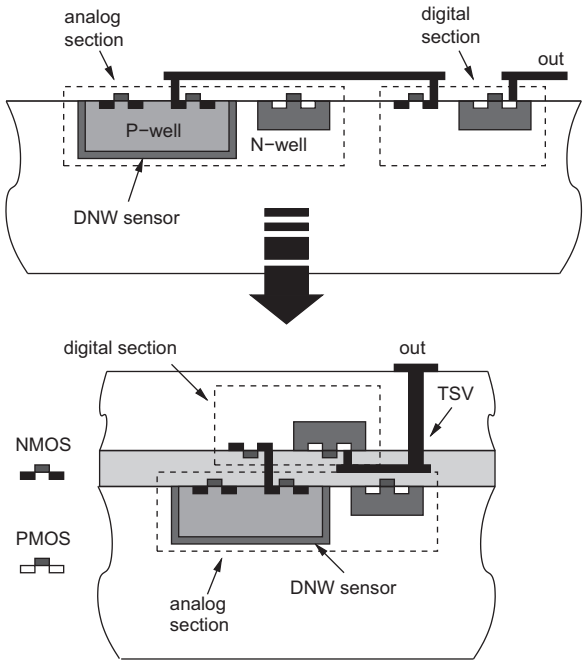

Fig. 2. Cross-sectional view of a DNW CMOS MAPS: from a planar CMOS technology to a 3D process.

2. Vertical integration technologies

The success of a vertical integration process relies upon three fundamental steps, namely

- fabrication of electrically isolated connections through the silicon substrate (through silicon vias, TSV);
- substrate thinning (below 50 μm);
- layer-to-layer alignment and mechanical bonding.

Different approaches have been proposed and are available for their implementation [6]. The technology cross-section shown in Fig. 1, in particular, points to the main features of the extremely cost-effective process provided by Tezzaron Semiconductor [7] which was used for the design of the SDR1 chip. The Tezzaron process can be used to vertically integrate two (or more) layers, specifically fabricated and processed for this purpose by Chartered Semiconductor in a 130 nm CMOS technology. In the Tezzaron/Chartered process, wafers are face-to-face bonded by means of thermo-compression techniques. Bond pads on each wafer are laid out on the copper top metal layer and provide the electrical contacts between devices integrated in the two layers. The top tier is thinned down to about 12 μm to expose the through silicon vias (TSV), therefore making connection to the buried circuits possible. Among the options available in the Chartered technology, the low power (1.5 V supply voltage) transistor option was chosen. The technology also provides six metal layers (including two top, thick metals), dual gate option (3.3 V I/O transistors) and N- and P-channel devices with multiple threshold voltages [8].

3. The SDR1 chip

The features of the Tezzaron/Chartered process have been exploited in the design of the SDR1 chip, which is based on the same readout architecture as the SDR0 monolithic sensor [2]. SDR1 is a two-tier, vertically integrated 240 × 256 MAPS matrix with a 20 μm pixel pitch, token passing binary readout architecture and the capability for storing two hits and the relevant 5-bit time stamps. The step from the DNW MAPS in a planar CMOS technology to its vertically integrated version is illustrated in Fig. 2, showing a cross-sectional view of a 2D MAPS and of its 3D translation. In the SDR1, the deep N-well sensor and the analog front-end are integrated on a different layer from the digital front-end (DFE). The main benefits deriving from such an approach can be summarized as follows:

- all the PMOS devices used in digital blocks are integrated in a different substrate from the sensor, therefore significantly reducing the amount of N-well area (and its parasitic charge collection effects) in the surroundings of the collecting electrode and improving the detector charge collection efficiency (CCE);
- although in the SDR1 chip the pitch is 20% smaller than in the SDR0 monolithic sensor (in which the pitch was 25 μm), the effective area available for device integration is larger (625 μm^2 in the SDR0 MAPS, 800−400 μm^2 for each tier—in the SDR1 sensor); this has been exploited to increase the functional density of the sensor (in particular, to implement the capability for double-hit storing) and to reduce threshold dispersion by designing large transistors where required (see Section 3.1);
- from the previous point it should be apparent that a better trade-off between integrated functionality and detector pitch can be achieved, yielding a smaller point resolution;
- separating the digital front-end from the analog processor and the sensor can effectively prevent digital blocks from interfering with the analog section and from injecting charge into the sensor through parasitic capacitive coupling; nevertheless, it is worth emphasizing here that the SDR0 test structures were not affected to a significant extent by this sort of problems.

The following sections provide a detailed description of the circuits integrated in the pixel cell, made up of 276 transistors, and of the general architecture of the detector.