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Large monolithic particle pixel-detector in high-voltage CMOS technology ☆

I. Perić *, C. Takacs

University of Heidelberg, Institute for Computer Science, Mannheim, Germany

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ABSTRACT

A large monolithic particle pixel-detector implemented as system on a chip in a high-voltage 0.35 μm CMOS technology will be presented. The detector uses high-voltage n-well/p-substrate diodes as pixel-sensors. The diodes can be reversely biased with more than 60 V. In this way, depleted zones of about 10 μm thickness are formed, where the signal charges can be collected by drift. Due to fast charge collection in the strong electric-field zones, a higher radiation tolerance of the sensor is expected than in the case of the standard MAPS detectors. Simple pixel-readout electronics are implemented inside the n-wells. The readout is based on a source follower with one select- and two reset-transistors. Due to embedding of the pixel-readout electronics inside the collecting electrodes (n-wells) there are no insensitive zones within the pixel matrix. The detector chip contains a 128×128 matrix consisting of pixels of $21 \times 21\,\mu m^2$ -size. The diode voltages of one selected pixel-row are received at the bottom of the matrix by 128 eight-bit single-slope ADCs. All ADCs operate in parallel. The ADC codes are read out using eight LVDS 500 MBit/s output links. The readout electronics are designed to allow the readout of the whole pixel matrix in less than 50 μs. The total DC power consumption of the chip is 50 mW. All analog parts of the chip are implemented using radiation-hard layout techniques. Experimental results will be presented.

1. Introduction and the chip architecture

Two particle pixel detector-prototypes implemented in a high-voltage CMOS technology have been described in Refs. [1,2]. The prototypes use lowly-doped n-well/p-substrate diodes as pixel sensors having the pixel readout electronics implemented inside the n-wells. The main portion of the signal originates from the depleted zones of the n-well diodes (10 μm thickness) where the signal charges are collected by drift. The feasibility of such a new detector concept has been demonstrated before [1,2]. The chip presented here is the first full-scale detector in the high-voltage CMOS technology that has such properties in terms of pixel size, number of pixels, readout speed, etc. that it can be applied in a real experiment.

Fig. 1 shows the block diagram of the chip. The chip contains a 128×128 matrix consisting of pixels of $21 \times 21\,\mu m^2$−size. The pixels are arranged as bricks in order to minimize charge sharing and in this way improve cluster SNR. The pixel structure will be explained later on. The pixels are readout in the rolling-shutter mode. For this purpose, a shift register is used to select the pixel row to be readout. Only one row is selected at a time. The voltages stored on the sensor diodes in the selected row are then transmitted to the end-of-column circuitry via vertical readout lines. The end-of-column electronics contain amplifiers, sample-and-hold circuits, ADCs and the readout registers. The sensor voltages are amplified, offsets subtracted, and the results digitized using 128 single-slope ADCs that operate in parallel. The ADC codes are read out using eight LVDS 500 MBit/s output links. The end-of-column electronics are designed to allow the readout of the entire matrix in less than 50 μs.

2. Pixel structure

Fig. 2 shows one pixel and its readout electronics. The simple pixel electronics are implemented directly inside the lowly-doped deep n-well. The electronics are based only on PMOS transistors. The NMOS transistors can be also used inside such pixels since the used technology allows placing of p-wells inside an n-well. However, a p-well takes relatively large space, and would introduce a large detector capacitance. On the other hand, PMOS transistors are less sensitive to ionizing radiation. Since our main goals were to achieve a small pixel size and a high radiation tolerance of the detector, we have chosen the only-PMOS implementation of the readout electronics.

The pixel electronics include a source-follower transistor Tsf used as the signal buffer, a select-transistor Tsel that connects the

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* Corresponding author.
E-mail address: ivan.peric@ziti.uni-heidelberg.de (I. Perić).

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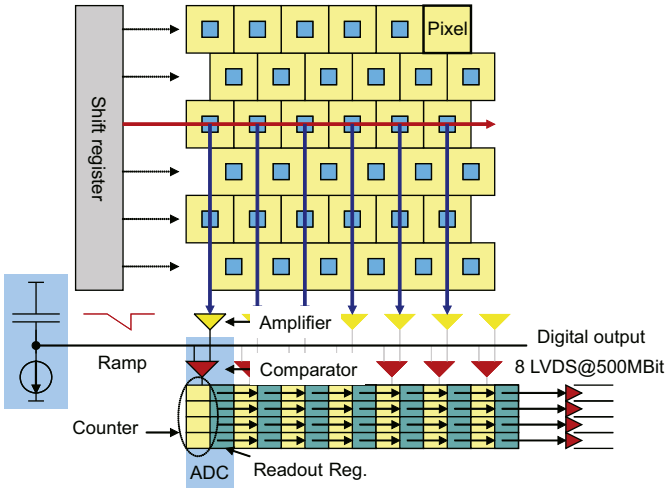

Fig. 1. Block diagram of the chip.

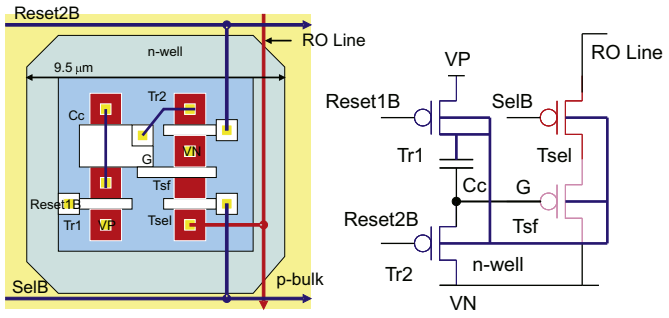

Fig. 2. Pixel electronics.

buffer to the readout line (RO line) and two reset transistors Tr1 and Tr2. The deep n-well is at the same time the signal collecting electrode and the bulk for the electronics. As PMOS transistor bulk, the n-well should have the potential higher or equal than transistor p+ diffusions. As collecting electrode, the n-well potential should be floating during the signal collection. Such an operation is controlled by reset transistor Tr1. During the short reset phase, this transistor shorts the n-well with the positive supply line VP and precharges it. Since the gate of Tsf (node G) has lower potential than the n-well, the connection between the n-well and the gate is established capacitively using capacitor Cc. Additional reset transistor Tr2 is needed to refresh node G potential from time to time.

3. Pixel operation

3.1. Reset

Fig. 3 shows the pixel cross-section. The lowly-doped n-wells in the used high-voltage technology can sustain a high reverse n-well/p-substrate bias. In our case, the p-substrate potential is typically by 60 V lower than n-well potential. (The used technology allows 120 V reverse bias.) In this way, a junction region of nearly 10 μm thickness is depleted.

In reset state, transistors Tr1 and Tr2 are on (Tr2 is not shown in Fig. 3). The n-well is shorted with VP (typically 3.3 V) and the gate of Tsf (node G) is shorted with bias line VN (2 V).

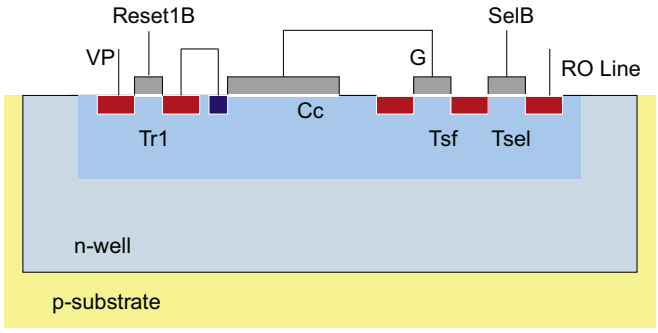

Fig. 3. Pixel cross-section.

3.2. Signal collection

During the signal collection period, transistors Tr1, Tr2 and Tsel are off. When a ionizing particle traverses the depleted region, the electrons and holes are separated by the strong electric field. (Due to the fast charge collection in the depleted zone and very limited charge sharing, significantly higher seed signals are measured than in the case of most standard MAPS detectors. We measure an average seed MIP signal of 1050 e. In theory, we expect a signal of about 800 e from the depleted zone. The remaining signal probably originates from the un-depleted substrate and is collected by diffusion.) After the charge collection, the potential of the n-well drops by typically 17 mV. This potential drop is determined by $\Delta V_{NW} = Q_s/C_d$, with Q_s the signal charge and C_d the total n-well capacitance. Since node G is capacitively coupled to the n-well, V_G changes by the same amount like V_{NW}. Hence, V_G has the following value after the signal charge collection

$$V_G = 2V - Q_s/C_d. \quad (1)$$

The coupling capacitor Cc is implemented as a thin-oxide PMOS capacitor.

3.3. Signal readout

Source follower transistor Tsf is connected to the readout line by closing select transistor Tsel. A PMOS current source connected to the readout line at the end of the column generates the bias current for Tsf. The potential of the readout line settles to the value $V_{ROL} \equiv V_{SIG} = V_G + V_{GS} = 2V - Q_s/C_d + V_{GS}$, V_{GS} is the gate-source voltage of Tsf (1). We should point out that V_{GS} depends on transistor dimensions and its threshold voltage. Since Tsf has nearly minimum size, the pixel-to-pixel dispersion of V_{GS} is relatively large. To alleviate this, there is the possibility to perform *analog double sampling* (ADS) readout: Potential V_{SIG} is stored on an capacitor in the end-of-column channel. After that, the pixel is reset by opening Tr1 and Tr2. V_G is precharged to 2 V and V_{ROL} takes the new value $V_{ROL} \equiv V_{RES} = 2V + V_{GS}$. The end-of-column amplifier amplifies then the difference $V_{SIG} - V_{RES}$ which is equal to the pure signal Q_s/C_d. Although it eliminates pixel-to-pixel base-line dispersion (*pedestal* dispersion), ADS does not eliminate the reset noise since the signal and the reset sample do not belong to the same frame and are not correlated.

3.4. Crosstalk issues

The fact that we have the readout electronics inside the collecting electrode has a few unwanted consequences. Particularly, every control signal, like the reset or select signal, couples *capacitively* to the sensor. We have neglected this effect in the previous discussion. We should mention that the crosstalk