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Design and performance of improved Column Parallel CCD, CPC2

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ABSTRACT

The Linear Collider Flavour Identification (LCFI) Collaboration is developing the sensors, readout electronics and mechanical support structures for the vertex detector of the International Linear Collider (ILC). High speed readout is needed to ensure that the occupancy due to the pair production background at the ILC is kept below the 1% level. In order to satisfy this requirement, Column Parallel CCDs (CPCCDs), Column Parallel Readout chips (CPRs) and Column Parallel Driver chips (CPDs) have been developed. The CPCCD has to operate at a clock frequency of 50 MHz, which represents a difficult technical challenge due to the large sensor capacitance. The design and performance of the second generation CPCCD sensors, CPC2, and the new driver chip, CPD1, which meet these challenging requirements, are described.

1. Introduction

The readout of the vertex detector (VXD) at the International Linear Collider (ILC) [1] represents a challenge due to the ILC beam structure and the massive beamstrahlung background. In the ILC one millisecond of intense collisions is followed by 199 ms of quiet time. The background originates from the electron–positron pairs radiated in the intense electromagnetic fields of the colliding bunches. The beam background dictates that during the collisions of a single bunch train, sensors are readout approximately 20 times maintaining the sensor occupancy below 1%. This corresponds to the frame readout rate of 20 kHz in the innermost layers per typically 1 MegaPixel frame, much faster than currently available in imaging CCD technologies. It is also essential for the vertex detector to be as light as possible, with a target thickness of 0.1% X_0 per layer, and to have the charge collection efficiency for ionizing particles close to 100%.

There are two main approaches to meet these challenging aims. The first one is to read out at maximum possible speed to satisfy the 20 frames in 1 ms requirement. This option is described in this manuscript in detail on example of Column Parallel CCD (CPCCD) [2–4]. The CPCCD sensors developed by the LCFI collaboration [5] allow shortening of the readout time of a classical CCD by the necessary factor. The CPCCD principle is explained in Fig. 1 and is, in essence, the readout of vectors in parallel instead of the sequential readout of a matrix. Continuous readout with a 50 MHz clock is needed to achieve the required 20 kHz frame rate, using a specialised readout chip, CPR [6,7], bump-bonded to the sensor. The same principle of fast readout is also pursued by CMOS MAPS [8] and DEPFET [9] sensors.

Another approach to satisfy the ILC specifications is to store the hit information at the pixel level which then can be read out at a slow rate during the quiet time. This approach is pursued by ISIS [10] and FAPS [11] sensor types. Similar approach has been under intense development also for ultra-high speed optical imaging [12]. A detailed comparison of different sensor options for the ILC vertex detector is presented in Refs. [5,13].

The fast and simultaneous charge transfer that occurs in all CCD columns means that the CPCCD clock must drive the substantial capacitance of the sensor at high speed. The time structure of collisions in the ILC requires the readout to last approximately 2 ms followed by a quiet time of 198 ms. The CPCCD presents a capacitance of about 50 nF between clock phases. This requires a clock drive current of about ± 20 A to ensure the clock drive voltage of ± 2 V is achieved. This manuscript describes the main design features and properties of the second generation CPCCD sensor, CPC2, produced by e2v [14] in 2007.

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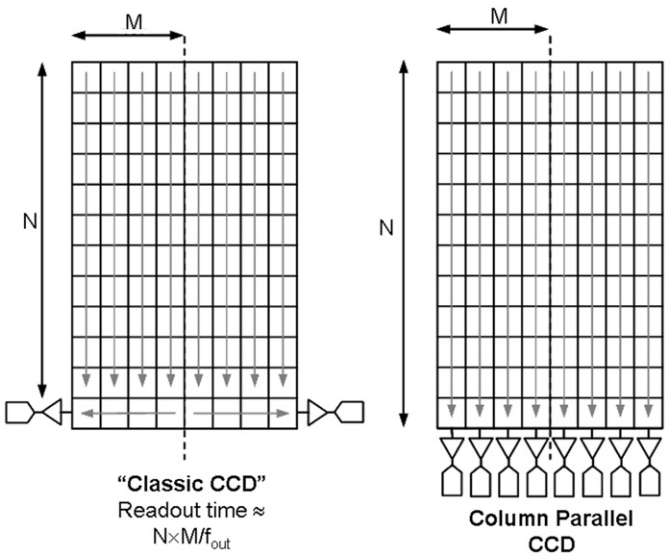

Fig. 1. Comparison of classic and column parallel CCDs.

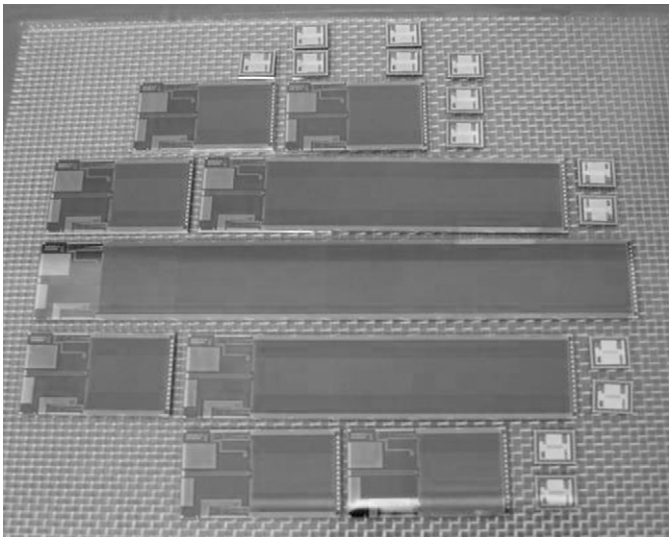

Fig. 2. Diced wafer of CPC2 sensors. The largest sensor has overall dimensions of $17.7 \times 104.0\ mm^2$. The small chips on the top and on the right are ISIS1 sensors described in [10].

2. CPC2 design

The CPC2 pixel size is 20 μm square with 750 columns, i.e. pixels per row. Several lengths of CPC2 have been manufactured using a stitching process. The "repeating" image section is 650 rows high. There are 20 additional rows of pixels in the "terminating section" with the readout components such that a total of (650*N*+20) rows of pixels are produced by photo-lithographically stitching together a chip with a terminating section and *N* image sections. Three sensor types with different lengths were produced with *N* equal to 1, 4 and 7. These sensors, shown in Fig. 2, were labelled accordingly: CPC2-10, CPC2-40 and CPC2-70. The longest sensor, CPC2-70, has 4570 pixels per column, corresponding to a sensitive area of $15.0 \times 91.4\ mm^2$ and has overall dimensions of $17.7 \times 104.0\ mm^2$. One end of the sensor was designed to accommodate two readout chips, one CPR1 [7] and one CPR2 [6], bump-bonded to the sensor.

The sensor operates with a two-phase clock with "standard" and "field enhanced" variants, the active lengths of the barrier and storage parts of each phase being 3.5/6.5 μm and 3.0/7.0 μm, respectively. In the "field enhanced" case the inter-phase implant has a trapezoidal shape, which creates fringing field in the direction of the transfer and also sideways towards the centre line of the pixel in order to speed up the transfer. Columns 1–183 and 568–750 are standard, whereas columns 184–567 are "field enhanced". The inter-column isolation region is 6.0 μm wide. There is a small gate overlap to ensure efficient charge transfer yet low inter-gate capacitance. Two variations of the epitaxial layer resistivity were used, one 25 μm thick with 100 Ωcm resistivity and another with 50 μm thickness and 1.5 kΩ cm resistivity. All measurements presented below were performed with the former option as only a few higher resistivity sensors were produced. Half of the columns give direct charge output (i.e. only an *n*+ node) and the other half implements outputs with source-followers. Bump-bonding connections are provided for the CPR1 or CPR2 chips for further charge or voltage amplification. Analogue readout of 12 columns is provided directly in three separate regions that cover the middle and two sides (columns 17–20, 374–377 and 731–734). These 12 columns have 2-stage source follower and all the rest have 1-stage source follower circuits.

The single stage circuit has a conventional buried-channel reset transistor, a surface-channel source follower transistor and a buried-channel on-chip load transistor. The same circuit is used for both the outputs to the CPR readout chips and the standalone analogue outputs and has a load current of 0.33 mA with a 2 V shift. The node capacitance is 33 fF with an overall responsivity of 4.4 μV/electron. The output impedance is 4 kΩ. The two-stage circuit is essentially the same as the single-stage circuit with the addition of a larger sized direct-coupled second-stage surface-channel source-follower transistor. An on-chip temperature sensing diode is located in the area under CPR1. Fig. 3 shows the schematic diagram of CPC2 output circuit for single stage and double stage output amplifiers. Values of the bias voltages used for all measurements described below are given in Table 1. The minimum peak-peak voltage used for the clocks, IØ1 and IØ2, was 2 V and the typical amplitude of the reset signal, ØR, was 10 V.

Two options for connecting the image section phases were explored. The first variant has metal electrodes with only a single clock bus-line on either side of the device and does not allow high frequency operation. This design can be accomplished with a single metal layer. In this version the image section bond pads on one side of the device are all IØ1 and those on the opposite side are all IØ2.

The "busline-free" variant uses two metal layers to connect to the polysilicon gates and to distribute the clock signal over the whole sensor area. It has the IØ2 connections formed as a sheet of first-level metal connecting the electrodes via the same contact holes used for the previous version. Suitable apertures are provided around the contact holes for IØ1 such that this phase can be connected with a similar sheet of second-level metal, the two metals being isolated from each other using a layer of polyimide. The contact holes for IØ1 are actually covered with small areas of first level metal to which the second-level metal connects through holes in the polyimide. The image section bond pads are now arranged in pairs, each having the clock pads for IØ1 and IØ2 located close to each other. Because the two clock currents always flow in opposite directions this approach allows cancellation of associated magnetic fields hence a higher frequency operation. This improvement comes at the expense of a higher capacitance. The yield of the busline-free design was considerably lower than that of the single metal design.

Fig. 4 shows a photograph of the busline-free design in the region adjacent to the area of the readout chip. Three rows of the CPR2 bump bonding contacts are visible in the bottom of