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Investigation of cutting edge in edge-on silicon microstrip detector

D. Vrtacnik*, D. Resnik, M. Mozek, B. Pecar, S. Amon

Faculty of Electrical Engineering, University of Ljubljana, Slovenia

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ABSTRACT

Investigation of cutting edge properties in edge-on silicon microstrip detector has been performed. An advanced approach for reducing dead layer thickness has been introduced. It consists of standard wafer sawing through entire wafer thickness, followed by dry chemical etching and thin layer passivation of the cutting surface. Proposed approach is developed in such a way that no additional photolithographic process steps and critical handling with individual chips are needed after detector fabrication. Results presented in the paper show that this approach results in effective reduction of cutting edge thickness down to 50 μm. Such reduction of dead layer thickness, together with applied efficient current termination technique resulted in substantial improvement of detector structure performance.

By described optimization of detector dead layer thickness, detection efficiency has been improved up to 15%.

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1. Introduction

Edge-on detectors play an essential role in various fields of X-ray diagnostics due to their high detection efficiency, which is close to 100%. In conjunctions with the X-ray tube they have found medical applications in spinal radiography for diagnosis of vertebral lesions [1,2] and in digital mammography [3–5]. Edge-on detectors are also efficiently used in experiments carried out with the synchrotron radiation, such as in planar radiography [6] and tomographic radiography [7,8].

Mammography is today the most effective examination for the diagnosis of the breast cancer [9]. Because radiation dose has to be kept at the lowest possible value, a medical image is always noise limited. Therefore, high contrast and spatial resolution are required in order to ensure early detection of the lesions. Edge-on silicon microstrip detector (SMD) fabricated with standard planar technology has inactive edge dead layer, which lowers quantum efficiency of the detector. Since the spectrum produced by a typical mammographic tube features intensity peak at relatively low energies, between 17.4 (Mo Kα) and 22.7 keV (Rh Kβ), it is of great importance to reduce the detector entrance window as possible.

Basically two different approaches have been used to reduce the dead layer thickness in edge-on SMD, i.e. by physical reduction of the cutting thickness [10,11] or by tilted illumination beside the undepleted region [12,13]. The reduction of the physical cutting edge is also of great importance in imaging applications with low-penetrating radiation and in applications where detector must be positioned as close as possible to a radiation beam, where so called “edgeless” detectors are used [11,14–17]. In cases where cutting is performed through the active area of the detector, it can only efficiently work at cryogenic temperatures.

Finished SMD wafer is usually diced into chips through the predefined scribe lines that are safely spaced outside of the device active area, typically ranging from 0.5 to 1.5 mm. A cut closer to the detector active area introduces a disordered region of high density lattice defects, dangling bonds, etc. at the cut surface. A significant part of these defects is electrically active, i.e. energy levels are created in the forbidden gap of the silicon. Due to the wide variety of these defects, their energy levels can be considered as to be continuously distributed between the valence and the conductive band, which increases the leakage current.

The main goal of this work was to improve the detection efficiency (signal-to noise-ratio) of the edge-on SMD for mammography, by reducing dead layer thickness of detector. For this purpose an advanced approach for reducing the dead layer thickness was applied consisting of standard wafer sawing with the diamond dicing blade through the entire wafer thickness, followed by the dry chemical etching and passivation of the cutting surface. The main idea is to apply the appropriate cutting edge treatment to the finished detector wafer so that no additional photolithographic steps or individual chip handling is needed. Results presented in the paper show that the proposed

* Corresponding author. Tel.: +38614768303; fax: +38614264630.
E-mail address: Danilo.Vrtacnik@fe.uni-lj.si (D. Vrtacnik).

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approach enables an effective reduction of the cutting edge thickness down to 50 μm, which was confirmed by measurements of the detector reverse current before and after the cut treatment.

2. Detector structure

Detector design, fabrication process and characterization are described in detail in our previous work [3,18]. In general, it is the one-sided $p^+n^-n^+$, AC coupled edge-on silicon strip detector with integrated FOXFET biasing structure. Detectors are fabricated in planar technology, adapted for high resistivity silicon substrates. Active detector area is 0.67 cm^2, with 140 strips of length 4 mm, width 50 μm and strip pitch of 100 μm. Schematic cross-section of detector structure is shown in Fig. 1.

Two guard rings (GR1 and GR2) consisting of p^+ layer surround the active area of the detector in order to reduce the electric field near the termination end of the strips. Usually, biasing of individual rings is carried out by the punch-through biasing [19]. In this case, the function of GR1, which is biased to the same potential as the detector biasing line, is to collect electrical carriers generated in its surrounding, which would otherwise be collected by the strips. The purpose of GR2 is to lower the electric field of GR1 and thereby to increase the breakdown voltage of the detector. In this case, if cut is safely applied, the cutting edge does not contribute to the detector reverse current as there is no potential drop across this cut.

In contrast to the above voltage termination structure (VTS), we allow that the entire detector bias is applied to the detector chip cut, and the resulting current is collected by the p^+-rings. Because this approach terminates the current, it is called current termination structure (CTS) and was first introduced by Ruggiero et al., [15]. This approach is efficiently used in "edgeless" detectors. In this case the outer ring GR2, called the current termination ring, collects the resulting current of the cutting edge while the clean-up ring GR1, placed between the detector active area and GR2, strongly reduces the influence of the current generated at the detector cutting edge on the leakage current of detector active area.

3. Detector efficiency

Two physical parameters limit the detector efficiency of edge-on SMD, the dead layer thickness (edge thickness) and the strip length.

If we assume that all X-ray photons absorbed in dead layer and those unabsorbed in the detector are lost, then the total detector efficiency, ε_T, is given by $\varepsilon_T = \varepsilon_E \times \varepsilon_D$ where $\varepsilon_E = e^{-x_E/\lambda}$, $\varepsilon_D = 1 - e^{-x_D/\lambda}$, λ is photon absorption length and x_E and x_D are detector dead layer thickness (distance from the cutting edge to the end of the strip) and detector strip length, respectively. Fig. 2 shows the total detector efficiency for $x_E = 50$ μm and strip length of 0.3, 1.0 and 5.0 mm, and edge efficiency, ε_E, for edge thicknesses of 50, 100 and 200 μm, versus incident X-ray photon energy. It can be seen that at least a few millimeters long strips are needed to absorb the majority of the 20 keV photons. For the dead layer thickness of 50 μm, detector strip length of 5 mm and energies lower then 20 keV, the limiting factor in achieving high total detector efficiency is the dead layer thickness. For energies above 20 keV the limiting factor is the detector strip length. In the case of 0.3 and 1.0 mm long strips, the benefit of 50 μm dead layer thickness on the total detector efficiency becomes negligible for the 20 keV photons. Presented analysis shows that 15% improvement of the detector efficiency could be expected if the edge thickness is efficiently decreased from a few hundred micrometers to 50 μm.

4. Experiment

After the detector was fabricated, both sides of the wafer were spin-on coated by the photoresist HPR504 (Arch Chemicals, Inc., USA). Resist baking temperature of 120 °C was used. Next, the wafer was mounted to the standard frame with the dicing blue tape (P/N 18074, Semiconductor Equipment Corporation, USA) and sawed through the entire wafer thickness. Cuts were performed by Disco DAD-2H/6T dicing saw, using the 25 μm wide diamond dicing blade, resulting in the cut width of approximately 40 μm. Detector chips were sawed at different distances, i.e. edge thicknesses, ranging from 80 to 220 μm from the end of strips, as shown in Fig. 3. The first cut (C1) was made at a distance of 220 μm from the strip end, i.e. on the distance equal to the wafer thickness. Due to the cut width of 40 μm, the final edge distance is 200 μm. Each of the remaining three cuts (C2, C3 and C4) was made 50 μm closer to the detector active area. Cuts C3 and C4 were made through GR2 and GR1, respectively. Thus, the cut C3 completely removes guard ring GR2 on the treated edge side, while the cut C4 only narrows GR1 (i.e. GR1 still remains terminated). Detector cuts at the left three sides, i.e. at the biasing side and at the remaining two sides of the detector were made at the safe edge distance of 320 μm.

After sawing some of the wafers (detector chip denoted as CE) received an additional isotropic plasma etch (denoted as CEE) and passivation (denoted as CEEP). The plasma etching and plasma passivation were performed in a standard parallel plate reactor with RF driven top electrode (13.56 MHz) and grounded bottom electrode. CF_4/N_2O gas chemistry was applied for plasma etching

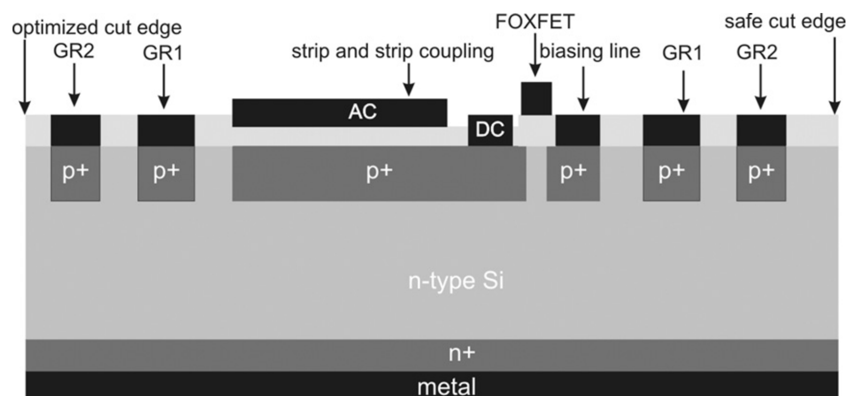

Fig. 1. Schematic cross-section of detector structure.

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