Nuclear Instruments and Methods in Physics Research A 629 (2011) 118–122

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

A CMOS compatible Microbulk Micromegas-like detector using silicon oxide as spacer material

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ARTICLE INFO

Article history:
Received 24 August 2010
Received in revised form
7 October 2010
Accepted 29 October 2010
Available online 10 November 2010

Keywords:
MPGD
GEMGrid
Microbulk
Micromegas
Silicon oxide
Timepix
CMOS post-processing
Microsystems
Above IC
Radiation detectors

ABSTRACT

We present a new Micro Pattern Gaseous Detector (MPGD) fabricated with nonpolymeric materials. The device structure is similar to a Microbulk Micromegas design, consisting of a punctured metal grid supported by a continuous perforated insulating structure. In this detector, the supporting structure is made out of silicon oxide. Devices were tested in He/iC_4H_{10} (80/20) and Ar/iC_4H_{10} (80/20) gas mixtures under ^{55}Fe irradiation. Gas gain of 20,000 and energy resolution below 13% FWHM were achieved. The CMOS compatibility of the fabrication process has been studied in Timepix chips as well as individual 0.13-μm technology CMOS transistors. Complete detectors have been fabricated on top of Timepix chips. In an Ar/iC_4H_{10} (80/20) gas mixture ^{55}Fe decay events were recorded operating the Timepix chip in 2D readout mode.

1. Introduction

Recently a new fabrication process for Micromegas [1] detectors, known as Microbulk [2], has been introduced. In this type of detectors, a punctured metal grid is not supported by sparse pillars, as in classical Micromegas, but by a continuous perforated structure. The holes in the metal grid and supporting structure are aligned but the latter ones are recessed. Inspired by this concept, in previous work we have fabricated a similar detector, called GEMGrid [3], on top of a Timepix chip [4]. In this detector, the supporting structure is made out of SU-8 photoresist [5]. Other polymeric materials are commonly used for the fabrication of MPGDs.

GEMGrid structures, in which the SU-8 has been replaced by benzo-cyclo-butene (BCB), a commercially available polymer from Dow Chemical, have been recently presented [6]. The device described in this paper has a GEMGrid design, but the SU-8 material is replaced by silicon oxide. For certain applications, this approach presents several benefits:

- Improved flatness of the metal grid.
- More accurate control of the geometry of the amplification gap.
- Easier feasibility of small amplification gaps (even in the micrometer range).
- Drastically reduced outgassing in the device.
- Likely reduced ageing (as compared with materials containing organic compounds).
- Improved moisture resistance.
- Better adhesion between metal grid and supporting structure (enabling wire bonding of the grid).
- Greater shock resistance and mechanical robustness.
- Higher thermal treatment tolerance than in the case of polymers.

Devices produced on dummy substrates have been tested in He/iC_4H_{10} (80/20) and Ar/iC_4H_{10} (80/20) gas mixtures at standard temperature and pressure under ^{55}Fe irradiation. Tests on Timepix chips and single 0.13-μm technology transistors were carried out to check the CMOS compatibility of the process. Complete detectors built on Timepix chips have also been tested under ^{55}Fe irradiation.

2. Fabrication process

The device fabrication process uses standard microfabrication techniques such as PECVD[1], DRIE[2], sputtering, wet etching and

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[1] Plasma enhanced chemical vapour deposition.
[2] Deep reactive ion etching.

0168-9002/$ - see front matter © 2010 Published by Elsevier B.V.
doi:10.1016/j.nima.2010.10.143

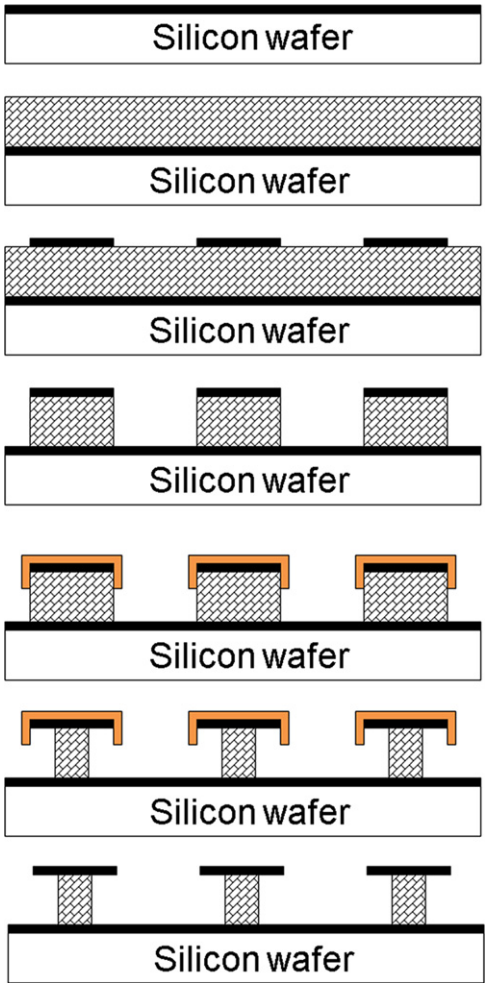

Fig. 1. Device fabrication process flow. From top to bottom: (1) Deposition of the metal anode on a silicon wafer. (2) PECVD deposition of a 32 μm thick silicon oxide layer. (3) Deposition and patterning of the aluminum metal grid. (4) Deep reactive ion etching of the silicon oxide. (5) Sputter deposition of a 50 nm thick Ti/W layer. (6) Underetch of the silicon oxide. (7) Removal of the Ti/W layer.

photolithography [7]. These techniques provide excellent precision and reproducibility, and allow integration of the devices on CMOS chips.

Before processing on Timepix chips, several tests were carried out on dummy substrates. Silicon wafers (4-inch diameter), containing nine $14 \times 14\,mm^2$ devices, were processed. The main fabrication steps, as shown in Fig. 1, are the following:

- Sputter deposition of the anode electrode (900 nm chromium) on a dummy silicon wafer. This electrode also acts as an etching stop layer.
- PECVD deposition of a 32 μm thick silicon oxide layer. The layer thickness was chosen for convenience with the rest of the process.
- Sputter deposition and patterning of a 1 μm thick aluminum layer.
- DRIE of the silicon oxide layer. The etching stops at the chromium electrode.
- Sputter deposition of a 50 nm thick Ti/W layer.
- Isotropic wet etch of the silicon oxide in a BHF[3] solution. Recessed silicon oxide holes with respect to the metal holes are obtained.
- Removal of the Ti/W layer in a hydrogen peroxide solution.

[3] Buffered hydrogen fluoride.

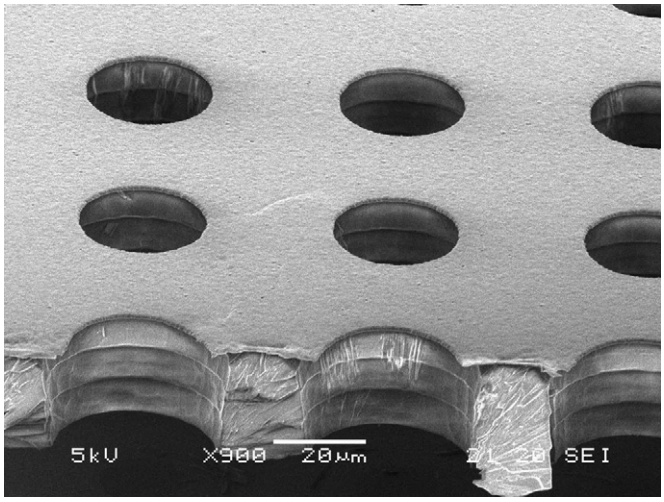

Fig. 2. Cross-section SEM picture of a finished device. The 1 μm thick aluminum grid is supported by a 32 μm thick continuous silicon oxide structure.

The metal grid hole diameter was 25 μm. The silicon oxide was recessed 6 μm with respect to the metal holes. From previous work, we established that recessed structures can reach higher gas gain than non-recessed structures [3]. The hole pitch was set to 55 μm, matching the pixel pitch of the Timepix chip.

The amplification gap thickness was set to 32 μm, which is thick enough obtain reasonable gas gain at atmospheric pressure. The thickness of the amplification gap can be controlled with high accuracy and made as small as few micrometers. For the DRIE of the silicon oxide layer, a 7 μm thick SU-8 photoresist mask is used [8], instead of the conventional approach of using a thick nickel or chromium mask [9,10]. Using a photoresist mask simplifies the process considerably. Good etching selectivity between silicon oxide and photoresist can be achieved. The etching rate of the silicon oxide is about 550 nm/min whereas for the photoresist it is about 100 nm/min.

The silicon oxide was underetched in a BHF solution. In this solution, the aluminum grid is roughened, therefore, prior to the silicon oxide underetch, a protective 50 nm Ti/W layer was deposited on top of the aluminum. Later on the Ti/W is removed in hydrogen peroxide. The possibility to use hydrogen fluoride vapour to underetch the silicon oxide is currently under investigation. Hydrogen fluoride vapour can etch silicon oxide selectively to aluminum and therefore the process can be simplified. Finally, the underetch will be extended to remove most of the silicon oxide material and leave small rhombus shape pillars in between the holes.

In a final step the wafer was diced into individual devices. Fig. 2 shows a cross-section SEM picture of a finished device.

3. Measurements

For the characterization of the devices, a dedicated chamber was employed. The chamber consists of an aluminum base plate and a cover to create a gas sealed volume where the devices are placed. A metal shielding box under the aluminum base contains the readout electronics. Connections can be made to the devices under test to supply the high voltage and read out the signals. More details about the chamber can be found in Ref. [11]. A wire bond connection was made to the grid to apply the high voltage. The anode was set to ground potential. For all the measurements the drift field was kept at a constant value of 1 kV/cm. The output of the grid was connected to an Amptek pocket multi-channel-analyzer for data recording.