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Pixel-level 8-bit 5-MS/s Wilkinson-type digitizer for the DSSC X-ray imager: Concept study

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ABSTRACT

A pixel-level 8-bit 5-MS/s digitizer for the DSSC X-ray imager utilizing the method of Wilkinson is presented. The timing information is generated column-wise by means of an 8-bit Gray-code counter. The 625-ps time stamps are distributed to the column pixels through 13-mm long shielded coplanar waveguides. Pixel-internal blocks comprise a sample-and-hold stage with current source for ramp generation, a temperature-compensated and supply voltage-stabilized reference circuitry, a comparator, a bank of eight receivers with latches for the time stamps, and control logic. These pixel-internal and global devices in 130-nm CMOS technology occupy 0.015 and 0.012 mm^2, respectively. The power consumption amounts to $\sim$800 μW at 1.2-V supply voltage. Taking the 0.8-V dynamic range into account, the simulated rms-noise voltage of about 240 μV corresponds to a signal-to-noise ratio above 70 dB. The differential and integral nonlinearity is expected to remain below 0.4 LSB and 1 LSB, respectively. All results promise the compliance with underlying requirements.

1. Introduction

The European X-ray Free Electron Laser (XFEL) facility, under construction in Hamburg, Germany, will provide uniquely intense and coherent short-pulse radiation in the X-ray regime. Up to 3000 pulses will be delivered with a minimal temporal spacing of $\sim$200 ns between each pulse and an overall repetition rate of 10 Hz. In order to utilize the fast 200-ns pulse separation and to investigate dynamics on that time scale at experiments, the development of a new area detector called DEPFET Sensor with Signal Compression (DSSC) [1] has been started last year. The DSSC X-ray imager is a mega-pixel camera combining a single-photon resolution capability at low photon numbers of up to 14 photons with a wide dynamic range of up to 6000 1-keV photons and a frame-rate capability of up to 5 MHz.

A unique feature of the DSSC imager is the nonlinear gain of the on-sensor integrated DEPFET digressively leaving a first gain region with an almost constant slope at input charges of around 4000 electrons. Below this value at least a 1-to-1 relation between the photon number N_{ph} and Analog-to-Digital Converter (ADC) count is needed for single-photon resolution, e.g. 274 electrons per ADC bin for a single 1-keV photon (1,000 eV/(3.65 eV/e^-)=274 e^-). Beyond that first gain region, the transfer function flattens increasingly so that the width of ADC bin 255 corresponds to 48 1-keV photons. This ADC count corresponds to $N_{ph}=6000$ 1-keV photons. In the whole dynamic range, the digitization noise remains below the fundamental noise component due to the statistical variation in the amount of photons impinging the sensor during the exposure time given by $\sqrt{N_{ph}}$ (Poisson limit) [1]. The photon-wise quantization for small signals gives us the opportunity to fit the ADC's bin size to a charge representing a single photon of known energy. But the bin size must be large enough to minimize the number of faulty entries into neighboring bins due to electronics noise. Taking the given DEPFET's transfer function into account, the needed number of bits only depends on the dynamic range. In our case, an ADC resolution of 8 bit is sufficient to cover the range of several thousand photons [1].

With a view on the XFEL-timing structure it is beneficial to store the recorded images inside the readout chip, since the X-ray pulses are delivered in 0.6-ms short bunch trains followed by a 99.4-ms long inter-train spacing. The in-pixel readout electronics of the DSSC imager comprises the signal chain from the sensor output to the frame-storing digital memory. Pixel-level ADCs can achieve higher Signal-to-Noise Ratio (SNR) and lower power consumption than other approaches, since the digitization is performed in parallel, close to where the signal is generated, and is operated at lowest speeds in comparison to pixel-sharing ADC approaches. Such approaches for on-focal-plane digitization were already successfully realized in 1994 [2] and allows to benefit from the conventional D/SRAM concepts. Ideally, an XFEL imager should be able to store all possible 3000 images per train, but space constraints according to the foreseen 200-μm pixel pitch limits the area available for the pixel-level memory. In contrast to an analog memory, a digital memory offers the lowest cell size, leads therewith to

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the highest frame-storage capacity, and is also much less sensitive on leakage-induced errors. Kleinfelder et al. demonstrated the large scalability potential of such a digital pixel sensor with an array of 352×288 ADCs and memories [3]. They reached already a high-frame rate potential of 10,000 frames per second utilizing a 0.18-μm CMOS technology. In the meantime, pixel-processing imagers come up opening new opportunities for SNR improvement and data reduction early in the signal chain. For example, Tyrrell et al. report on a readout chip implemented in 90-nm CMOS technology and hybridized to a 256×256 30-μm pitch HgCdTe detector array [4] demonstrating the future potential of the digital pixel-sensor approach.

A system-level model of the DSSC X-ray imager was already presented in Ref. [5] discussing the needs for the SNR as well as for further design-relevant parameters like gain- and offset-adjustment granularities under special circumstances of the exemplarily chosen experimental class of X-ray Photon Correlation Spectroscopy (XPCS). Taking these boundary conditions as summarized in Section 2 into consideration, this paper presents the concept of an adequate ADC suitable for pixel-level integration. A brief survey of state-of-the-art ADCs and imagers utilizing column- and pixel-level ADCs is given in Section 3. Section 4 presents our ADC concept for the DSSC X-ray imager and deals with circuit and layout issues of the ADC's main building blocks. First experimental results are summarized. The last section gives a conclusion.

2. ADC requirements

Considering a full-scale voltage of 0.8 V, an 8-bit ADC would allocate a single 1-keV photon to the first ADC bin with a bin size of 3.125 mV. In the ideal case, the entries caused by single-photon and four-photon events must be located in the center of bin one and four, respectively. These examples are depicted by Fig. 1 (vertical and horizontal dotted lines). Noise broadens these peaks to Gaussian-shaped curves and leads to faulty entries in neighboring bins. Once the peak broadening becomes comparable to the ADC's bin size, the system response becomes very sensitive to offset and gain errors. These cases are illustrated by the lower two graphs in Fig. 1. A positive offset consistently shifts the peaks away from the corresponding bin centers to higher values. A too high gain value leads to a nonlinear peak shift. The single-photon peak is still located in the first ADC bin, whereas the four-photon peak has almost totally been shifted out of the fourth bin. Therefore, all three limitations, noise, gain and offset errors, cause wrong counts marked as hatched areas in Fig. 1. This demonstrates the importance of the minimization of offset and gain errors as well as of the noise level. Consequently, a trimming procedure must be carried out for each pixel in order to obtain a uniform response over the whole camera.

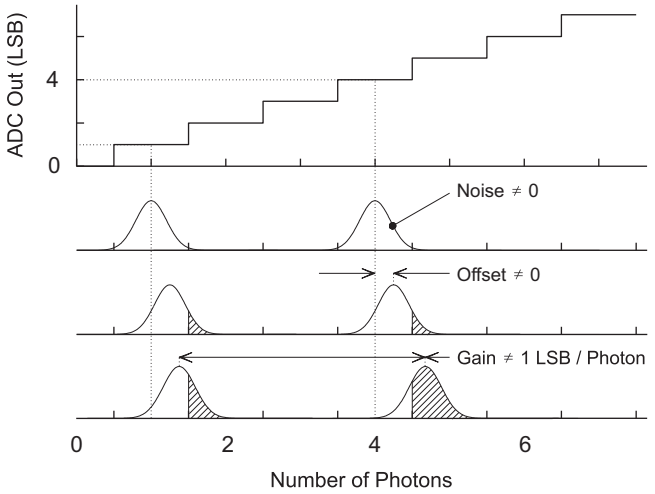

Fig. 1. First gain section of the system-transfer function for 1-keV photon numbers below 10. The lower three diagrams show noise-, offset-, and gain error-related trimming issues.

In order to get an impression on the influence of these limitations in real experiments, the system-level model was applied to images recorded during a XPCS experiment using an 801×801-pixel CCD [5]. This experiment exhibits images at a mean-count rate of 3.4 photons per pixel and a maximum number of 38 photons per pixel permitting the examination of the influence of the primary ADC quantization. Gaussian-shaped disturbance functions were implemented with relative standard deviations representing the bin size-relative offset and optimum gain-relative gain errors. The simulations were made for 1-keV photons representing a bin size of ~ 274 e$^-$ at a noise level of 57 e$^-$. Difference images between the measured XPCS-input images as seen by the CCD and output images of the system-level model of the DSSC X-ray imager were calculated. Some of these difference images are exemplarily depicted in Fig. 2, where each black dot represents a wrong pixel count with an error of one photon. The offset-related difference images (top) are regarded as free of gain errors and vice versa. The curves denote the error rate (number of pixels detecting a wrong photon number relative to the total pixel number) of the border areas free of regular structures (background) versus the relative standard deviation. These regions are of particular interest for performance tests, because the pixel rate is limited to a few photons. An offset-standard deviation of 5% results in an almost homogeneous distribution of faulty pixel with an amount of only 1.2% for the background (grey curve). In case of gain disturbance (black curve), a comparable value of faulty-pixel rate for the background is already reached for a standard deviation of 10%. But, in order to limit the 1-σ fluctuations of the maximum detectable photon number to $\sim 10\%$, a gain-trimming granularity of 10% is also required. Dealing with both disturbances simultaneously and applying the full calibration scheme [5], a total error rate as marked by the fully black circles can be achieved. An rms-noise value of 57 e$^-$ representing a bin size-related $SNR = 274$ e$^-$/57 e$^- \simeq 5$ leads to an error rate of only 1%. As indicated by the lower fully black circle (16 e$^-$), lower noise levels will finally lead to a pixel-error rate well below one percent. This range of values is sufficient for the requirements of XPCS experiments. In summary,

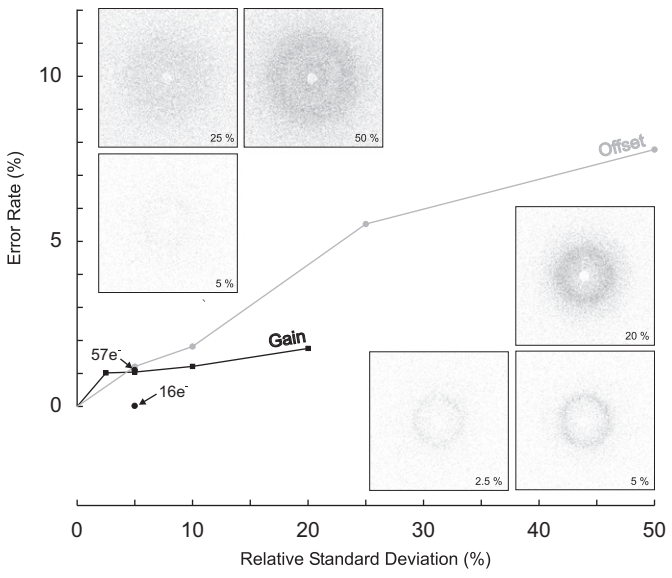

Fig. 2. Error rate of the background areas versus the relative standard deviation of offset (grey) and gain (black) at 57-e$^-$ noise level. Black cycles represent the sum-error rates finally achievable after system calibration for noise levels of 57 e$^-$ and 16 e$^-$.