Nuclear Instruments and Methods in Physics Research A 609 (2009) 122–128

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Planar transformers for column parallel CCD clock drive

B. Hawes [a], D. Cussans [c], C. Damerell [b], E. Devetak [a], J. Fopma [a], R. Gao [a], J. Goldstein [c], T. Greenshaw [d], S. Hillert [a], N. Kundu [a], A. Nomerotski [a,*], C. Perry [a], K. Stefanov [b], S. Thomas [b], S. Worm [b]

[a] University of Oxford, Particle Physics, Denys Wilkinson Building, Keble Road, Oxford OX1 3RH, UK
[b] STFC Rutherford Appleton Laboratory, Harwell Science and Innovation Campus, Didcot OX11 0QX, UK
[c] University of Bristol, Tyndall Avenue, Bristol BS8 1TL, UK
[d] University of Liverpool, Oliver Lodge Laboratory, Liverpool L69 7ZE, UK

ARTICLE INFO

Article history:
Received 18 July 2009
Accepted 30 July 2009
Available online 21 August 2009

Keywords:
Column parallel CCD
Planar transformer
Substrate bounce

ABSTRACT

The LCFI Collaboration is developing the sensors, readout electronics and mechanical support structures for the Vertex Detector (VXD) of the International Linear Collider (ILC). High-speed readout is needed to ensure that the occupancy due to the pair production background at the ILC is kept below 1% level. In order to satisfy this requirement, Column Parallel CCDs (CPCCDs) and Column Parallel Readout chips (CPRs) have been developed. The CPCCD has to operate at a clock frequency of 50 MHz, which represents a difficult technical challenge due to the relatively large sensor capacitance. The design and performance of planar transformers, which can be used to provide the required 20 A clock current, are described.

1. Introduction

The readout of the Vertex Detector (VXD) at the International Linear Collider (ILC) [1] represents a challenge due to the ILC beam structure and the massive beamstrahlung background that it will produce. The background originates from the electron–positron pairs radiated in the intense electromagnetic fields of the colliding bunches. Assuming the sensors of the VXD must be read out once the occupancy reaches 1%, the required rate in the innermost layers is 20 kHz per typically 1 MegaPixel frame, orders of magnitude faster than currently available technologies. A solution that allows shortening of the readout time of a classical CCD by the necessary factor is being developed by the Linear Collider Flavor Identification (LCFI) collaboration [2]. The principle of a Column Parallel CCD (CPCCD) [3] is explained in Fig. 1 and is, in essence, the readout of vectors in parallel instead of the sequential readout of the elements of a matrix. Continuous readout with a 50 MHz clock is needed to achieve the required 20 kHz frame rate, using a specialised readout chip, CPR2A [4], bump-bonded to the sensor.

The fast and simultaneous charge transfer, which occurs in all CCD columns means that the CPCCD clock must drive the substantial capacitance of the sensor at high speed. The time structure of collisions in ILC requires the readout to last approximately 2 ms followed by quiet time of 198 ms. The CPCCD presents a capacitance of about 40 nF between clock phases. This requires a clock drive current of about ± 20 A to ensure that the clock drive voltage of ± 2 V is achieved. This paper describes investigations on the use of planar transformers built on a Printed Circuit Board (PCB) to drive the detectors.

LCFI is currently testing the second-generation CPCCD sensor, CPC2, produced by e2V [5]. The CPC2 pixel size is 20 μm square with 750 pixels per row. Several lengths of CPC2 have been manufactured using a stitching process. The longest sensor, CPC2-70, has 4570 pixels per column and overall dimensions of $17.7 \times 104.0\,\mathrm{mm}^2$. The sensor operates with a two-phase clock with the active lengths of the barrier and storage parts of each phase in pixels 3.5 and 6.5 μm, respectively. The inter-column isolation region is 6.0 μm wide. The silicon wafers used for CPC2 production are 500 μm thick and have a p-type epitaxial layer of 20 μm depth.

There are two options for connecting the image section phases. The first variant has metal electrodes with only a single clock busline on either side of the device and does not allow high-frequency operation. The "busline-free" variant uses two metal layers to connect to the polysilicon gates and to distribute the clock signal over the whole sensor area. This approach allows a higher frequency operation by minimizing the effective inductance at the expense of a higher capacitance. Two methods of producing the clock drive were investigated, one using a custom CMOS inverter, CPD1, capable of driving the required current [6] and another using a planar transformer described in detail in this paper. Fig. 2 shows a photograph of a CPC2-40 sensor on a motherboard with two planar transformers.

* Corresponding author.
E-mail address: A.Nomerotski@physics.ox.ac.uk (A. Nomerotski).

0168-9002/$ - see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2009.07.103

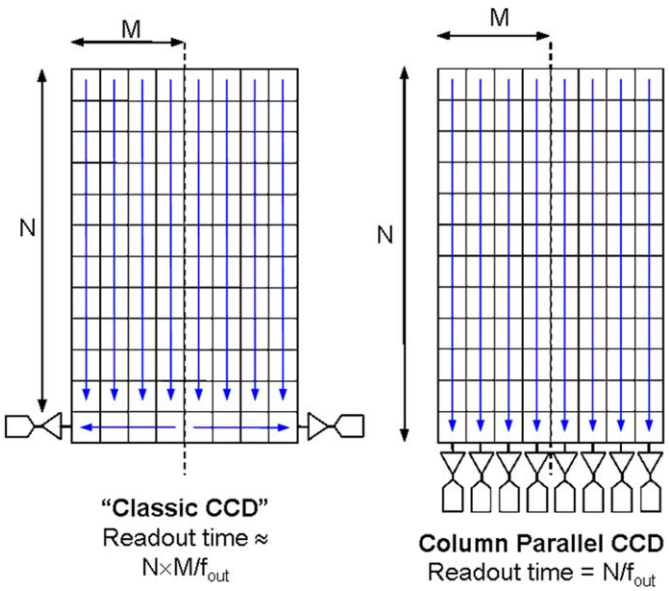

Fig. 1. Comparison of classic and column parallel CCDs.

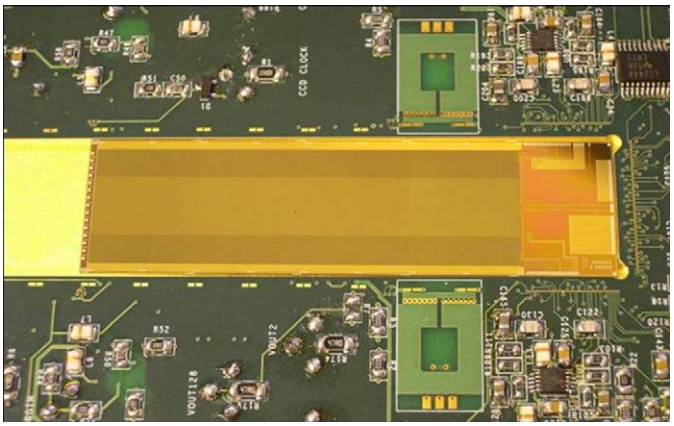

Fig. 2. CPC2-40 chip on a motherboard driven by two planar transformers.

2. Planar transformer

The use of planar transformers incorporated into a printed circuit board is not new and much literature exists, including the work of Hurley and Duffy who have published several papers on planar magnetic structures on ferromagnetic substrates, e.g. [7]. It is, however, not possible to use ferrites in components to be used in an ILC detector, which will have to function in an overall magnetic field of up to 5 T, sufficient to saturate a ferrite core. Hui et al. [8] have investigated coreless planar transformers. The principal difference in the present work lies in the need for operation at high current of up to 20 A in the 50 MHz region, which places severe restrictions on the allowable parasitic effects. Multi-layer devices have been designed to help reduce these.

To achieve the required speed, the total secondary leakage plus output connection stray inductance should be no more than that required to resonate with the 40 nF capacitance at 50 MHz, i.e. about 250 pH. Allocating one-third each to the transformer, the output side tracking and the wire bonds gives about 80 pH for each. This is a very difficult specification when one considers that 1 mm of straight wire has an inductance of about 1 nH. The situation is eased by the fact that the two clock planes are driven in anti-phase so that by suitably balancing the layout of the tracks, their magnetic fields may be made to partially cancel, reducing the inductance.

The impedance presented by a 40 nF capacitance at 50 MHz is about 0.08 Ω and this needs to be transformed to a level which can more easily be driven. A 12:1 turns ratio in a transformer would correspond to 12 Ω and 16:1 to 20 Ω of mostly reactive impedance. These are manageable and the designs evaluated are in these ratios. The transformer is a planar structure built on the nine layers of a multi-layer printed circuit board, which also carries the readout and control electronics for testing the CPCCD. The transformer has four primary windings, connected in series, and five single-turn secondary windings connected in parallel by multiple vias. As will be shown below, details of the transformer output to the chip connections are as important as the transformer design.

3. Transformer connections

The very low residual inductance necessary for the full clock speed of 50 MHz means that the design must use methods usually needed only at much higher frequencies. Analytic approaches, although available [7], have limited use when the performance is determined largely by parasitics. The present designs have been arrived at by electromagnetic simulation and measurement rather than calculation. Software is now available which facilitates this [9–11].

The bond pads available for connection to the clock planes of the first-generation CPC2 chips are not ideally arranged. There are two pads of $140 \times 340\,\mu m^2$ arranged side by side. These are repeated at intervals of 6.3 mm along the edge of the chip.

A single bond wire, 2 mm long and with a loop 0.5 mm high will have an inductance of about 2.2 nH, already greater than the present requirements. The fact that the clock signals are driven in anti-phase does make it possible to partially cancel the fields and hence reduce the inductance.

Fig. 3 shows two sets of five bond wires connected to the CPC2 pads as described in the previous paragraph.

The impedance matrices calculated using FastHenry [10] at 5 and 50 MHz are presented in Table 1 as self-inductance, M_{11}, and mutual inductance, M_{12}, terms in units of R [mΩ]+L [pH].

The resistance per phase is $(11.0-(-0.3))=11.3\,m\Omega$ and the residual inductance is (530–198)=332 pH at 50 MHz. The real component of the mutual impedance is due to the proximity effect caused by the re-distribution of current in a conductor due to the

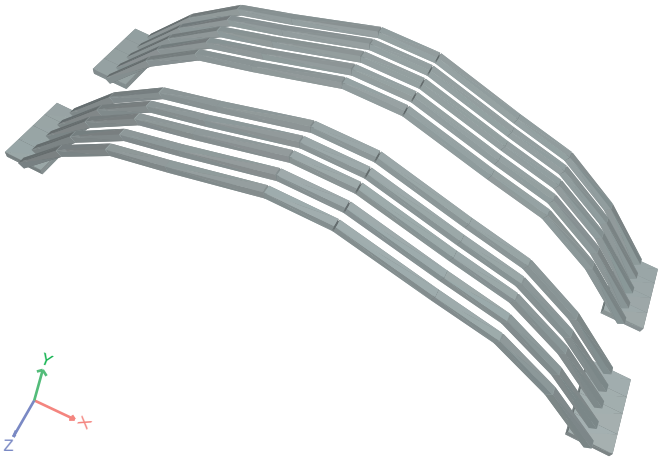

Fig. 3. Two sets of five bond wires on CPC clock pads.