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LLRF systems for subharmonic buncher system of BEPCII Linac

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ABSTRACT

The linear accelerator (Linac) completed in 2007 for the upgrading project of the Beijing Electron Positron Collider (BEPCII) provides 1.89 GeV electrons and positrons for the storage rings. BEPCII Linac decides to update the bunching system and adopts two-bunch operation to enhance beam quality and injection rate as its second update phase. Two subharmonic bunchers will be used in this project: one operates at 142.8 MHz and the other operates at 571.2 MHz. Each subharmonic buncher consists of the bunching cavity, power source, LLRF system and other related subsystems. This paper mainly describes the LLRF systems for the subharmonic buncher systems (SHB).

1. Introduction

The BEPCII Linac will be operated with two bunches injection mode [1] in which two electron bunches are initiated by pulsing the electron gun twice during one microwave pulse. A beam pulse coming from the electron gun has a pulse width of 1 ns (full width at half maximum). By passing through the bunching system, which includes the two subharmonic bunchers (SHB1 and SHB2) and one S band buncher, the electron bunch length is expected to be 10 ps wide exiting the S band buncher [2]. Fig. 1 shows the RF system for future BEPCII Linac where the SHB1 and SHB2 are newly installed. K1…K16 are the 16 Klystrons. A0…A6, A55, A7…A54 are the 56 accelerating tubes. About 13 SLAC Energy Doubler (SLED) have been used for increasing the beam energy. IΦA unit that drives the klystron is used to adjust the input signal's amplitude and phase. The Six Reference Signal Generator synthesizes the drive frequencies for the electron-gun pulsing system (17.85 MHz), the Linac subharmonic bunchers (142.8 MHz for SHB1, 571.2 MHz for SHB2), S-band buncher (2856 MHz), the S-band accelerator (2856 MHz) and the storage rings (499.8 MHz).

2. Subharmonic buncher system

SHB1 or SHB2 consists of a buncher cavity, one power source and an LLRF system. Fig. 2 is the diagram of one subharmonic buncher. The reference signal is from the Six Reference Signal Generator. The Solid State Amplifier (SSA) is the main RF power source. LLRF system that drives the SSA not only controls the RF amplitude and phase in the buncher cavity but also communicates with PC. An Experimental Physics and Industrial Control System (EPICS) Input and Output Control (IOC) program runs on the PC for remote communication and monitoring. The output of LLRF is continuous wave and the SSA output is pulse modulated by synchronization pulse from the timing system with width about 70 μs. Some parameters of the buncher cavities, the requirements for the power sources and the LLRF systems are shown in Table 1 [3].

3. LLRF systems

The LLRF system is used to measure and control the RF field in the RF cavity [4,5]. Due to the heating effects, the SHB buncher cavities have inherent problems such as expansion and resonance frequency shifting, so some measures must be taken to keep the buncher cavities' RF amplitude and phase within a limited range. Minimizing the duty cycle and controlling the watering system's temperature close to 45 °C are not enough because the RF field in

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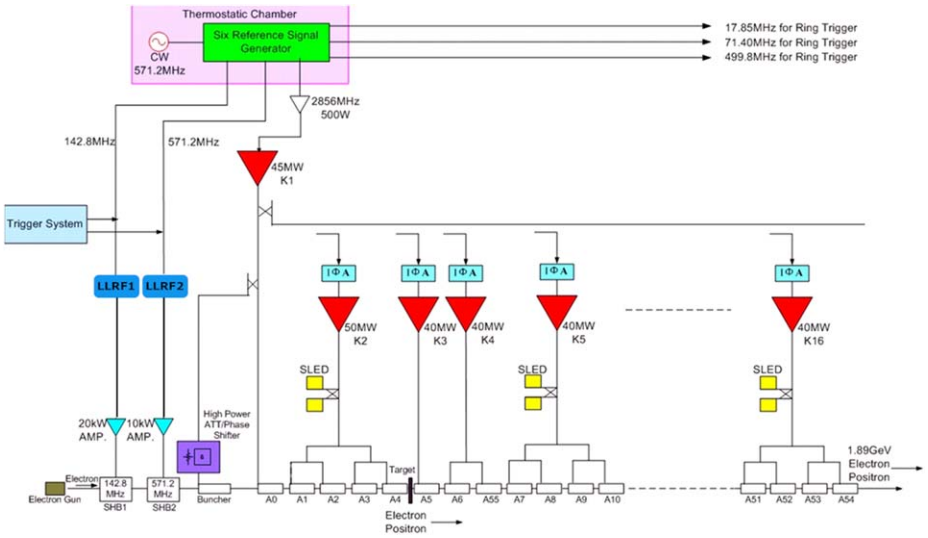

Fig. 1. Layout of the RF system for the future BEPCII Linac.

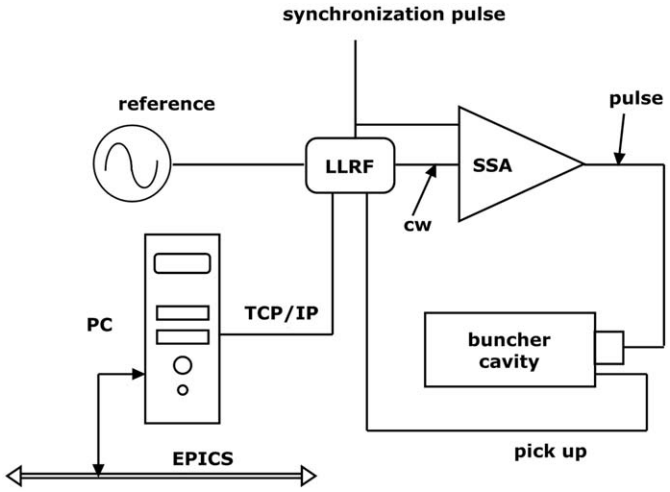

Fig. 2. Block diagram of one subharmonic buncher.

SHB cavities are always changing. On the other hand, the phase drift and slow changes in the RF power caused by variation of operation environment will affect the system's stability. We use an LLRF system to control the RF amplitude and phase pulse by pulse. The components and the control algorithm in SHB LLRF systems are described as follows.

3.1. Components

SHB1 or SHB2 LLRF system has a frequency synthesizer, one digital signal process board and an up convertor. The frequency synthesizer shown in Fig. 3 synthesizes the clocks for the digital signal process board and local oscillator frequency for up and down conversions, four channels RF signals can also be down-converted to an intermediate frequency at 17.85 MHz.

Fig. 4 shows the digital signal processing development board from Altera Corporation [6]. There are two high-speed ADC and DAC, one high-performance Altera FPGA chip and some accessorial devices on the board. The clock signals from frequency synthesizer have a frequency of 71.4 MHz. The IF signal sampled by ADC, I (In-phase) and Q (Quadrature components) output from DAC are all at the frequency of 17.85 MHz. One channel ADC on the board samples the signal down-converted from the cavity pick-up signal while the other one standby, $\underline{I}$ and Q channel are the inputs of up-convertor. Verilog and C++ codes have been programmed into the board to accomplish feedback control and remote communications. These parts for SHB1 and SHB2 are identical.

The up-convertor (shown in Fig. 5) in the LLRF system uses AD8345 by single side modulation to up-convert the intermediate frequency I and Q from FPGA board to RF signal with going through a band pass filter connected to one 20 dB gain amplifier. Output of the up-convertor drives the SSA.

Table 1
Some parameters and requirements for SHB.

Subsystem	Parameters/ requirements	SHB1	SHB2
Buncher cavity (tested parameters)	Operation frequency	142.8 MHz	571.2 MHz
	QL	4046	5391
	Coupling factor	1.04	0.97
	Tuning range	240 kHz	1.2 MHz
	Gap spacing	40 mm	30 mm
	Power required	14 kW	7 kW
SSA (requirements)	Max output power	20 kW	10 kW
	Pulse width	~70 μs	~70 μs
	Phase variation in pulse	1°	1°
	Power flatness	2%	2%
	Repetition rate	50 Hz	50 Hz
	Input frequency	142.8 MHz(cw)	571.2 MHz(cw)
LLRF system (requirements)	Amplitude stability	1.5%	1.5%
	Phase stability	1.5°	1.5°

3.2. Algorithmic and datapath in FPGA

SHB LLRF systems mainly compensate the slow variations of RF amplitude and phase in buncher cavities while ignoring the slight