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Development of X-ray CCD camera system with high readout rate using ASIC

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ABSTRACT

We report on the development of an X-ray charge-coupled device (CCD) camera system with high readout rate using application-specific integrated circuit (ASIC) and Camera Link standard. The distinctive $\Delta\Sigma$ type analog-to-digital converter is introduced into the chip to achieve effective noise shaping and to obtain a high resolution with relatively simple circuits. The unit test proved moderately low equivalent input noise of 70 μV with a high readout pixel rate of 625 kHz, while the entire chip consumes only 100 mW. The Camera Link standard was applied for the connectivity between the camera system and frame grabbers. In the initial test of the whole system, we adopted a P-channel CCD with a thick depletion layer developed for X-ray CCD camera onboard the next Japanese X-ray astronomical satellite. The characteristic X-rays from ^{109}Cd were successfully read out resulting in the energy resolution of 379(±7) eV (FWHM) @22.1 keV, that is, $\Delta E/E = 1.7\%$ with a readout rate of 44 kHz.

1. Introduction

X-ray CCD (charge-coupled device) camera has achieved primary roles in X-ray astronomy thanks to its following performances in imaging spectroscopy. The energy resolution has reached up to ~130 eV (FWHM) [1–3], which is almost the Fano limit (~120 eV), and spatial resolution is the order of 10 μm. The quantum efficiency is satisfactorily high in the wide energy range of almost two orders of magnitude from 0.3 to 12 keV. Their timing resolutions, however, is typically several seconds when we read out the entire region of CCD with frame transfer. Therefore, only a small fraction of the imaging area is read out and/or we give up continuous exposure to avoid photon pile-up when we observe some bright astronomical objects.

The poor timing resolution results from the limited readout pixel rate of typically $\leq$ 100 kHz and a few number of readout nodes per chip. Higher pixel rate leads to higher noise level because of the limited signal to noise ratio, and the conventional electronics with discrete integrated circuits require much power consumption and large space. Hence the straightforward way to improve pixel rate is to increase the number of readout nodes with subsequent electronics including application-specific integrated circuit (ASIC).

Recently some payloads for astronomical satellites have equipped with ASICs for low power consumption, low noise, and small size [4–6]. In fact Meidinger et al. [7] reported that their CCD camera system with a thick (450 μm), fully depleted pnCCD and ASIC chip proved the low readout noise of 2e$^-$ and fast pixel rate of 13 MHz. All of the above ASICs, however, only manipulate analog signals or barely have a discriminator. To suppress the potential readout noise affects the analog signals more strictly, we, therefore have been developing an ASIC with an analog-to-digital conversion capability and placed it just next to the CCD.

Furthermore, we have developed a prototype of the high speed X-ray CCD camera system employing the Camera Link standard for connectivity between X-ray CCD and a frame grabber in the ground test. This paper reports on the results of the initial test of our system using a CCD with a large number of pixels.

After the simple description of ASIC and our CCD camera system in Sections 2 and 3, respectively, we will briefly explain the initial results of readout tests (Section 4), followed by summary (Section 5). Indicated errors below mean 90% confidence level, unless otherwise mentioned.

2. Description of the ASIC

2.1. Specification

Basic circuit configuration of our ASIC (hereafter we call it MND01) is the same as that of MD01 [8]. Here we abstract

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its specification that characterizes our CCD camera system. Four identical circuits process the output signals of CCD simultaneously. Each circuit consists of preamplifier, 5-bit DAC and two $\Delta\Sigma$ modulators [9]. It was implemented through Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm CMOS process and then 3 mm^2 bare chip is packed into 15 mm^2 quad flat package (QFP). The mask layout of MND01 is shown in Fig. 1. It works with 3.3 V power supply for analog and digital circuits.

We show the signal process of MND01 in Fig. 2. Input signal is first amplified with adjustable gain from 0.6 to 16 in nine steps. The signal from CCD is composed of reset, floating, and signal level. The voltage gap between the latter two levels depends on the amount of electrons transferred by CCD. In most cases, however, there is a gap between these levels even when there is no input signal, which results as an offset in "energy-pulse height" relation. To control this offset and effectively use MND01's dynamic range, we put an offset to the signal level by 5-bit digital-to-analog converter. Then $\Delta\Sigma$ modulator [10] takes oversampling for voltages of these levels and integrates them (V_{int}). We measure the voltage gap by integrating the two levels with opposite polarity. The digital signal is output simultaneously as sampling. When V_{int} exceeds the reference voltage (V_{ref}), the output is "1" and V_{ref} is subtracted from V_{int}. Hence the number of bit "1" in the output bit stream depends on the amplitude of input signal. In our case, the total number of sampling, which is equal to the number of output bit stream, is 155 per pixel. This multiple sampling by the $\Delta\Sigma$ modulator shifts the majority of the quantization noise above the signal band in the frequency spectrum. Finally, the bit stream is decimation-filtered in subsequent circuits and finally we obtain the 12-bit decimal value. We have determined the weighting coefficients for each bit in the decimation filter by simulations of our circuits (Fig. 6 in Ref. [8]) to upgrade the frequency response as low-pass filter and improve signal-to-noise ratio of the signals. We summarized the above specifications of MND01 in Table 1.

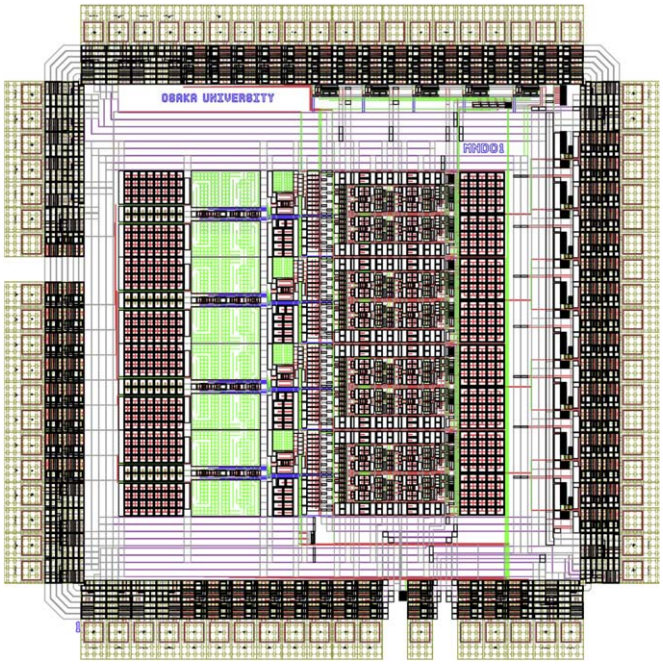

Fig. 1. Mask layout of MND01 with a size of 3 mm^2 square. It was made through 0.35 μm CMOS process of TSMC. Four identical circuits are positioned in vertical direction and they process the signals from a CCD simultaneously.

2.2. Unit performance

We describe here the results of the unit tests of MND01. Pseudo CCD signals with constant input voltage were input for all channels simultaneously; 800 pixels data were read out and then we shifted the input voltage in 20 steps throughout the dynamic range from −20 mV to +20 mV. Readout rate was set from 19.5 kHz to 1.25 MHz in multiples of 2. The power supply to MND01 is 3.3 V throughout this paper, unless otherwise specified.

First, we measured the power consumption by comparing the current in the printed circuit board (PCB) between the case when MND01 is mounted and that when it is not on the PCB. As the top panel in Fig. 3 shows, we tested two cases with supplied voltage of 3.3 and 3.5 V. Although the current increases with the readout rate, the power consumption of the entire chip is less than 120 mW even in the case of 1.25 MHz. The difference of the power between the two cases reflects the subsequent current discrepancy. In the middle panel in Fig. 3 we show the noise performance of MND01. The standard deviation of the decimal values was measured from the data of 800 pixels for each input voltage and we took the average of 20 sets of different voltages. We confirmed that the noise level is suppressed to be no more than 40 μV at the pixel rate of <80 kHz and 70 μV until the rate of 625 kHz. Integrated non-linearity (INL) was also measured as

Table 1
The specification of MND01.

Bare chip size	3 mm × 3 mm
Packaged chip size	15 mm × 15 mm
Number of channels	4
Power supply	3.3 V (digital and analog)
Process	TSMC 0.35 μm CMOS process

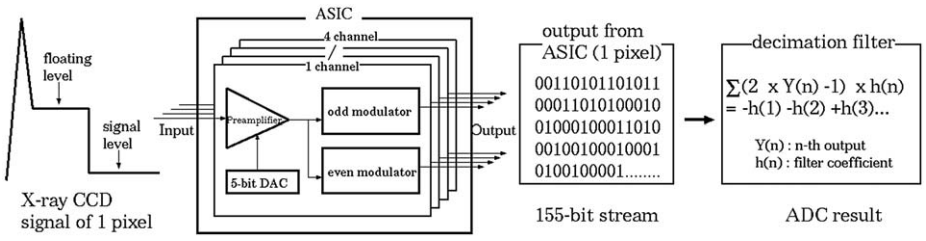

Fig. 2. The diagram of the signal processing. Input signals from CCD are at first amplified with adjustable gain. Simultaneously we put specific offset to the signal level in order to make use of dynamic range of MND01. Finally $\Delta\Sigma$ modulators convert analog signal of one pixel to digital 155-bit stream. Two modulators ("even" and "odd") work by turns to improve the readout rate.