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Caliste 64, a new CdTe micro-camera for hard X-ray spectro-imaging

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ABSTRACT

In the frame of the Simbol-X mission of hard X-ray astrophysics, a prototype of micro-camera with 64 pixels called Caliste 64 has been designed and several samples have been tested. The device integrates ultra-low-noise IDeF-X V1.1 ASICs from CEA and a 1 cm^2 Al Schottky CdTe detector from Acrorad because of its high uniformity and spectroscopic performance. The process of hybridization, mastered by the 3D Plus company, respects space applications standards. The camera is a spectro-imager with time-tagging capability. Each photon interacting in the semiconductor is tagged with a time, a position and an energy. Time resolution is better than 100 ns rms for energy deposits greater than 20 keV, taking into account electronic noise and technological dispersal of the front-end electronics. The spectrum summed across the 64 pixels results in an energy resolution of 664 eV fwhm at 13.94 keV and 842 eV fwhm at 59.54 keV, when the detector is cooled down to $-10\,^{\circ}$C and biased at -500 V.

1. Scientific context

1.1. Simbol-X mission

The Simbol-X mission is a hard X-ray space telescope. It is currently undergoing a phase B with the French and the Italian space agencies. This 20 m focal length observatory will be composed of two satellites flying in formation. One carries the grazing incidence mirror to focus X-rays until 80 keV. The other satellite carries the detector payload. This focusing technique improves sensitivity and angular resolution by two orders of magnitude compared to the current instruments above 10 keV. The core scientific objectives of Simbol-X are black holes physics and particle acceleration mechanisms [1,2].

The detection set consists of three detector units. The Low-Energy Detector is a silicon drift detector with DEPFET readout, also called "Macro Pixel Detector" [3]. It covers the energy range from 0.5 to 20 keV. The High-Energy Detector installed below the first detector is equipped with CdTe detectors to be efficient from 4 to 100 keV. The third unit is an active shielding to reject background (unfocused photons and protons) by temporal coincidence.

1.2. The High-Energy Detector

Requirements for this instrument come from both imaging and spectroscopy constraints. A pixel pitch of 625 μm is necessary to properly sample the ~3 mm diameter HEW point spread function. The 12 arcmin field of view requires a detector array of 64 cm^2. Detector material uniformity is also essential to guarantee high imaging quality. The spectroscopic performance baseline of 1.2 keV fwhm at 60 keV is driven by the study of supernovae. To build explosive nucleosynthesis models in young supernovae, a key parameter is the abundance of the ^{44}Ti isotope, visible through the 68 and 78 keV lines emitted in its decay chain. The best detector candidate until now is the Schottky CdTe detector from Acrorad with Al–Ti–Au anode because it demonstrated excellent uniformity and spectroscopic performance when associated with very low-noise electronics [4,5].

Imaging requirements lead to a High-Energy Detector with 16384 pixels. Each pixel has its own readout channel. One of the main technological difficulties is to integrate the front-end electronics. The solution contemplated is to put side by side 64 independent cameras of 256 pixels, with their front-end electronics below their 1 cm^2 detector. Caliste prototypes are designed to match Simbol-X scientific requirements while taking into account this strong constraint of integration.

The first step of this development is the design, the fabrication and the validation of a micro-camera with 64 pixels of 1 mm pitch called Caliste 64. Section 2 presents the design of this hybrid and

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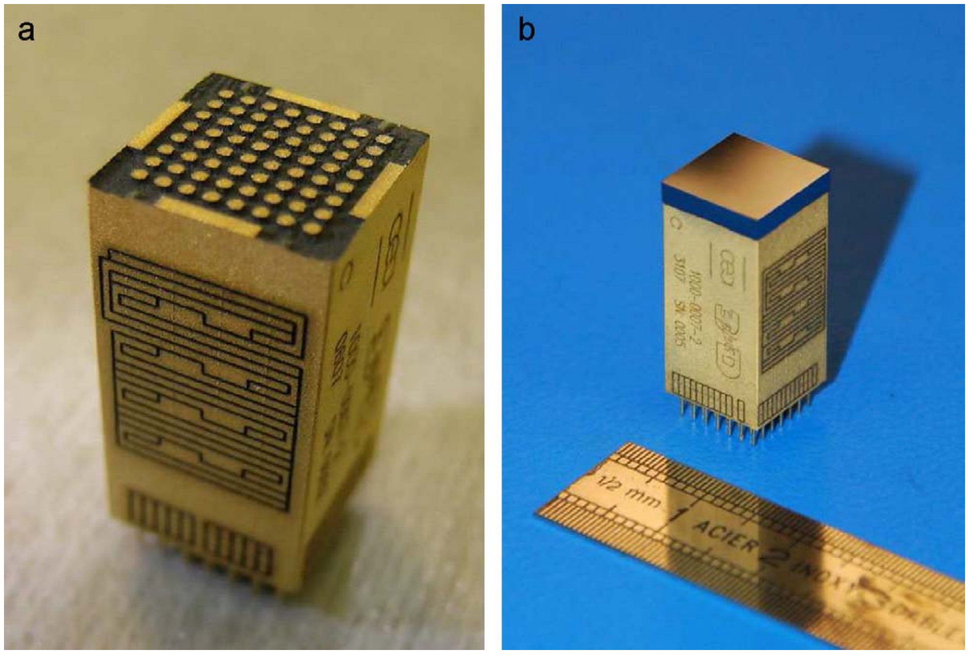

Fig. 1. (a) $10 \times 10 \times 18\,mm^3$ electrical body of Caliste 64, featuring four ASIC IDeF-X V1.1 responsible for reading out two rows of 8 pixels each. (b) Caliste 64 camera with a 2-mm-thick Schottky CdTe detector of 64 pixels.

the way to operate it. Section 3 illustrates the performance of the camera, in terms of imaging, spectroscopy and particle time-tagging.

2. Caliste 64 design and tests

2.1. Hybridization

Caliste 64 is the integration of a 64-pixel Cd(Zn)Te detector with full-custom ASICs to read out each pixel independently. Four ASICs called IDeF-X V1.1 with 16 analog channels are stacked perpendicular to the detection surface [6]. They are molded in an epoxy resin and connected to a 7×7 pin grid array to form the electrical body of the camera. The top surface of the block is prepared by laser ablation to receive an 8×8 pixel sensor (Fig. 1a). A Cd(Zn)Te of 1 or 2 mm thick with a segmented anode is reported on top of the electrical body. The complete camera stands in a $1 \times 1 \times 2\,cm^3$ volume (Fig. 1b). The whole fabrication, mastered by the 3D Plus company, respects space standards [7]. Since electronics is utterly integrated below the $1\,cm^2$ detector, several Caliste 64 cameras can be placed side by side to constitute a large focal plane. Todate, three cameras with Al Schottky CdTe detectors have been tested and six electrical bodies have been validated to receive CdTe or CdZnTe detectors.

2.2. Set-up

A Caliste 64 sample can be tested in the same set-up, before and after mounting a detector. The electrical body or the complete camera is placed in the thermal enclosure for electric or spectroscopic tests. Electric tests aim at validating the performance of the low-noise front-end electronics. To simulate amounts of charges created by the Cd(Zn)Te detector, fast voltage steps are brought by a test pin of the Caliste 64 interface and are injected through the calibrated injection capacitances of the four ASICs. Spectroscopic tests aim at studying the quality of our detectors in terms of uniformity, dark current level, stability in time with respect to the temperature and the bias voltage. A $100\,\mu m$ gold wire is glued on the top planar cathode to supply the bias voltage. An ^{241}Am source with a collimator is placed above the crystal (Fig. 2). For both tests, as soon as at least one channel detects a charge event, the Caliste sample sends a trigger outside the vessel. A board equipped with an FPGA performs the readout sequence of the hit pixels and sends data packets to the computer through a Spacewire link. The FPGA is also in charge of configuring the ASIC (low-level threshold, peaking time, pixel disabling, etc.) according to the user commands.

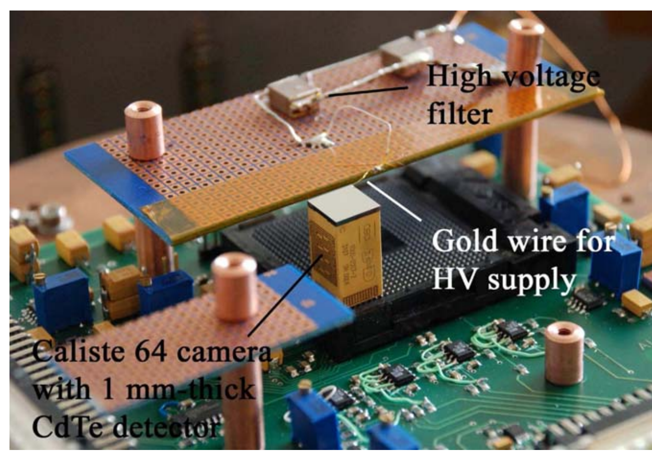

Fig. 2. Caliste 64 camera in the thermal enclosure of the test bench. High voltage is supplied by a $100\,\mu m$ gold wire glued on the planar cathode of the 1-mm-thick detector. A (non-visible) plate with an aperture is placed above the camera to receive the Am source.

3. Caliste 64 performance

3.1. Imaging

The anode is an array of 8×8 pixels of $900\,\mu m$ side, processed by photolithography. The pixels are separated by a $100\,\mu m$ gap