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Design of fundamental building blocks for fast binary readout CMOS sensors used in high-energy physics experiments

Yavuz Değerli *

CEA Saclay, IRFU/SEDI, 91191 Gif-sur-Yvette Cedex, France

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ABSTRACT

In this paper, design details of key building blocks for fast binary readout CMOS monolithic active pixel sensors developed for charged particle detection are presented. Firstly, an all-NMOS pixel architecture with in-pixel amplification and reset noise suppression which allows fast readout is presented. This pixel achieves high charge-to-voltage conversion factors (CVF) using a few number of transistors inside the pixel. It uses a pre-amplifying stage close to the detector and a simple double sampling (DS) circuitry to store the reset level of the detector. The DS removes the offset mismatches of amplifiers and the reset noise of the detector. Offset mismatches of the source follower are also corrected by a second column-level DS stage. The second important building block of these sensors, a low-power auto-zeroed column-level discriminator, is also presented. These two blocks transform the charge of the impinging particle into binary data. Finally, some experimental results obtained on CMOS chips designed using these blocks are presented.

1. Introduction

Since the early 1990s, CMOS image sensors built using standard commercially available CMOS processes earned more and more customer interest thanks to its characteristics like miniaturization, low power and low cost [1]. The growing demand for CMOS image sensors demonstrates its successful applications in the domain of visible light photon detection.

Meanwhile, in the domain of high-energy particle physics, some future applications and their experimental conditions require to integrate the detecting elements with the front-end electronics on the same silicon substrate. The recent advancements of CMOS sensors make it a promising candidate. The use of CMOS sensors for charged particle tracking was firstly proposed by the Strasbourg group [2]. In these monolithic sensors, 3-T photodiode pixels together with simple analog serial readout were used.

In the application of visible light domain, the photons reach a depth of only a few micrometers inside the CMOS sensor because of their low energy. The charge collection principle of high-energy ionizing particles is quite different from the detection of visible light photons (Fig. 1). The high-energy particles at the Ionizing Minimum (MIPs) penetrate through the sensor and therefore electron–hole pairs will be generated along the particle's track. Only a small part of the active volume near the charge collecting n-well/p-epi diode is depleted. So, the electrons generated in the epitaxial-layer diffuse thermally underneath the readout electronics, until they reach the low-potential region in the n-well. A near 100% fill factor [3], as required in particle tracking applications, is then obtained. The doping gradient results in a potential minimum in the middle of the epi-layer, limiting charge spread. The thickness of the epi-layer is typically about 10 μm, and the signal collected from an MIP traversing the detector is only a few hundreds of electrons. In the case of a high-resistivity substrate without epi-layer, the charges diffuse more laterally and vertically, the n-well/p-substrate diode collects less charge consequently. Note that, in twin-tub (double well) processes, PMOS transistors being fabricated in n-wells, only NMOS transistors can be used in this type of pixel aiming at charged particle detection. The pixel pitch needed in this domain is often above 10 μm.

Full digital output data and on-chip real time data processing are required for future high-energy experiments like the vertex detector of the future international linear collider. In this paper, design details of the basic components of a fast, binary readout CMOS Monolithic Active Pixel Sensor (MAPS) will be presented. The all-NMOS pixel presented in Section 2 is the first key element of such a monolithic sensor. The second basic block, a high-speed, low-power auto-zeroed discriminator (comparator) realized at the end of each column will be presented in Section 3. These two blocks transform the charge of the impinging particle into binary data.

The blocks described in this paper were successfully used in fast binary readout prototypes designed in two different CMOS

* Tel.: +33 169 0861 65; fax: +33 1 69 0 83 147.
E-mail address: degerli@cea.fr

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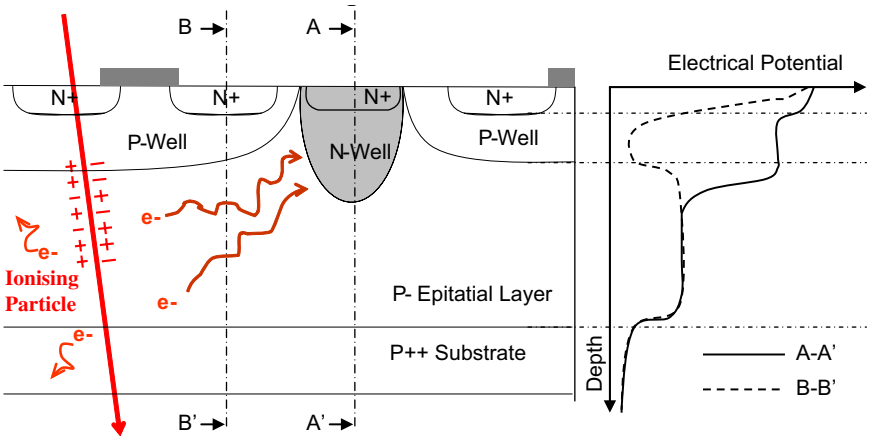

Fig. 1. Principle of charge collection in photo-diode type CMOS sensors.

processes: The first on the TSMC 0.25 μm CMOS digital process without analog options, and the second on the AMS 0.35 μm CMOS process with different substrate types. Some experimental results obtained on these chips will be given in Section 4.

2. Pixel design

To integrate on-chip data sparsification (or zero suppression) with fast readout, the classical CMOS 3-T photodiode pixels need several modifications. Firstly, (correlated) double sampling (DS) is required to suppress the reset noise of the small diode capacitance. Also all the pixel-to-pixel and column-to-column process related transistor offset non-uniformities (fixed pattern noises-FPN), which would be of the order of the signal generated by an impinging particle, have to be suppressed inside the pixel. The maximum achievable Charge-to-Voltage Conversion Factor (CVF) is limited to $\sim 20\,\mu V/e^-$ with n-well/p-epi diodes in mainstream CMOS processes. This is not sufficient to overcome the residual noises, even after correction with DS. In order to increase the *Signal-to-Noise* ratio (S/N), the detector signal must be amplified *as close as possible* to the charge collecting diode.

2.1. Reset noise suppression

Some methods have been presented in the literature to reduce or remove the reset noise of 3-T photodiode pixels [4–10]. While these methods are theoretically efficient, they need often long durations of the reset for a good reduction of noise, and in practice present high FPN due to the increased number of transistors and capacitors used inside the pixels.

The reset noise suppression method proposed in [4] consists of the use of a serial capacitor, a switch and a source follower (SF) to store the reset level of the detector capacitance in the pixel. This pixel could be used for charged particle tracking, if some issues are addressed. The high readout rates required in most of the high-energy physics experiments (integration times of at least a few tens of μs/frame) and the 100% fill-factor property of the pixel with an n-well/p-epi diode give the opportunity to store easily the reset level of the detector on an in-pixel analog memory. The pixel presented here is based on this architecture (Fig. 2), but several important changes were made to the pixel presented in [4]. Firstly, a simple n-well/p-epi diode with reset transistor as the detector was used instead of a photodiode with readout floating capacitor separated by a transfer gate. In fact, as the transfer transistor operates in the sub-threshold regime, a charge transfer problem occurs in this pixel [11,12]. Very long integration times are needed for an efficient transfer, which are not possible in our applications. To increase the CVF and improve the *S/N*, an amplifying stage was used instead of the first SF. A basic common-source (CS) stage with diode-connected NMOS load is the simplest way to realize this amplifier (Fig. 3). The CS stage is switched instead of continuous bias of the SF, in order to save power consumption. The small-signal voltage gain of this amplifier is given by

$$v_{out}/v_{in} \cong -g_{m1}/g_{m3} \quad (1)$$

where g_m is the transconductance of the MOS transistor. The simulations show that a gain of about 10 can be obtained keeping a reasonable dynamic range. To remove the offset voltages of the output SF, its offset is sampled externally during the measure of reset level of the detector on the in-pixel serial capacitor. To increase the readout speed, the gate voltage of the output SFs bias transistor is switched. This limits signal variations on the column bus by avoiding the bus capacitance discharge. In this pixel, all the signal swings were reduced to maximize the readout speed.

The key points of the design are as follows:

- The reset transistor should remain in linear region for a fast reset (called 'hard reset').
- The MOS capacitor (MOSCAP) should remain in inversion for better linearity.
- The CS stage should remain in appropriate operating region.
- The second switch transistor should remain in linear region for a fast reset.
- The SF should remain in appropriate operating region.

The choices of the diode voltage V_{r1} and the clamping voltage V_{r2} are very critical to satisfy these requirements.

2.2. Noise sources

The main temporal and FPN sources of this pixel are well known: All the noises generated by the first switch transistor (thermal noise, low-frequency noise, channel charge injection, clock feed-through etc.) and sampled on the detector capacitance are removed through in-pixel correlated double sampling (CDS) circuitry. The offset of the CS stage is also removed through CDS. It should be noted that the CDS doubles its thermal noise power [13], and the $1/f$ noise is not removed. However, as a high CVF is obtained close to the detector, input referred noise remains small. The thermal noise generated by the second switch and sampled on the MOSCAP is not removed, but this noise is small compared to the other temporal noises. The channel charge injected by this switch and the clock feed-through are removed through DS