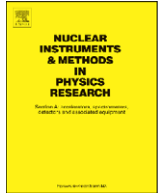




Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Custom pulse generator for RPC testing

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ARTICLE INFO

Available online 3 January 2009

Keywords:

RPC
Resistive plate chambers
Front end electronics
Pulse generators
Ionizing gas detectors
TOF

ABSTRACT

We present a pulse generator able to generate pulses statistically similar to the ones produced by RPC cells. The device generates up to four arrays of fast and narrow random-like pulses. Polarity, maximum amplitudes, widths and pulse rate in each channel may be modified independently in order to simulate different RPC setups and environments. This portable and cost-effective pulse generator is a versatile instrument for testing FE-Electronics and different real detector features related with the signal propagation inside the detector. It has been developed in the framework of the ESTRELA¹ project of the HADES experiment at GSI.

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1. Introduction

Resistive plate chambers (RPCs) [1] have found a very broad use in nuclear and particle physics experiments due to the outstanding performances they offer at an affordable price in comparison with other technologies. Many experiments that are now being built or designed will use this kind of detectors either for trigger or for TOF purposes [2]. The time resolution that RPCs offer at a low cost per unit area make them the ideal detectors for experiments in which big surfaces or detecting volumes have to be covered. RPCs also accept a broad variety of cell designs, sizes and readout electronics philosophies.

In the framework of the HADES experiment at the GSI (Darmstadt, Germany) [3], a timing-RPCs wall is being designed in order to perform low-level trigger tasks at the low polar angles region of the spectrometer. As part of an HADES upgrade for heavy ions collisions, we are developing RIGEL, an on-purpose device able to simulate pulses statistically similar to the ones produced by real RPC cells. Such a tool is interesting from the point of view of testing the amplifying electronics and also in RPC detector studies [6]. The Front End Electronics (FEE) that is being designed for ESTRELA [4,5] has one preamplifier stage based on the BGM1013 analog amplifier, with a gain of around 31 dB. The

narrow electron peak of a typical signal has a rise time of about 500 ps and a width of 5 ns.

2. Main features and applications

The development of the pulse generator, called RIGEL (RPC-like signals GEnerator for Laboratory testing), started with the aim to provide a customized and versatile laboratory tool as an alternative of using more sophisticated and expensive equipments. As a further advantage RIGEL is able to provide trains of almost random pulses with several widths and amplitudes like in a real detector. Its small size and low price are other two important features that make RIGEL a very interesting device.

In summary the main features offered by RIGEL are:

- To provide random-like pulse patterns.
- To allow the tuning of pulse amplitudes, widths and rates in order to reproduce different RPC cell architectures and environments.
- To provide up to four output channels (like an array of real detectors).
- To provide a common start pulse, propagated via adjustable delays to the four output channels, for timing analysis.
- Low power consumption.
- Small size and simple electronic device.
- Affordable cost.

The main application of RIGEL is to facilitate the tasks of testing timing FEE. The idea is shown in Fig. 1. The square output pulse provided by the pulse generator can be passed through a passive

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¹ ESTRELA (Electrically Shielded Timing RPC Ensemble for Low Angles) is part of the upgrade of the HADES experiment at GSI with the aim of constructing an RPC-based time-of-flight wall that will cover around 8 m² in order to cope with the high particle multiplicities expected for heavy nuclei collision systems such as Au+Au.

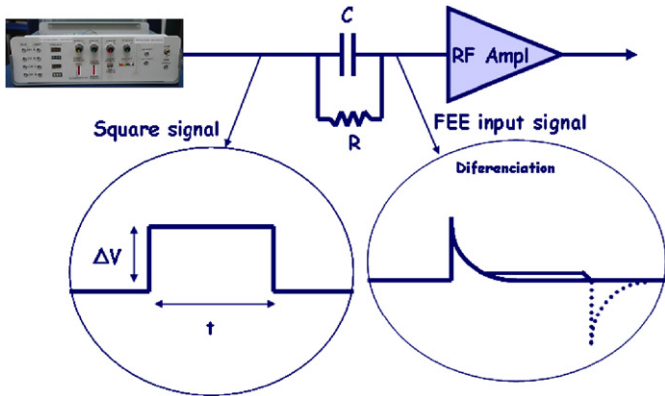


Fig. 1. Set up for injecting charge pulses to the electronics.

RC network to produce a signal with a known charge that may be injected into the preamplifier of the FEE.

The charge (Q_e) contained in the resulting signal depends only on the value of C and the ΔV of the square signal, and can be easily calculated through Eq. (1). The effect of the ionization tail produced on a real detector can be simulated by the use of R , which adds to the differentiated signal a constant charge that remains all the duration of the pulse. The total charge (Q_i) produced due to this effect depends also on the width and amplitude of the pulse, and is calculated as given in Eq. (2):

$$Q_e = \Delta VC \tag{1}$$

$$Q_i = (\Delta V/R)t \tag{2}$$

The passive network is not included inside the pulse generator and should be added externally. It is advisable locate the network at the end of the signal cable, next to the preamplifier to reduce the noise pick up. Even better, it could also be integrated into the FEE board as a test input. The external RC network is also more versatile, since the values can be selected for each specific requirement.

The setup proposed in Fig. 1 allows performing systematic studies of the behavior of the electronic for fixed or variable charge input signals, and also characterizing the electronics in terms of minimum and maximum input charge. Working at different input frequencies it is also possible to characterize the maximum rate of the system for different cases, it is even possible to generate pile-ups. The *START* output provided by RIGEL allows measurement of time resolution of the FEE. In case of multiple FEE channels, crosstalk studies are also possible.

RIGEL can also be used as a usual signal generator for analyzing real detectors features. Injecting a known pulse or pulses pattern to a detector or array of detectors may allow analyzing how signals propagate or spread out over the detectors, providing a very useful tool for RPC detector diagnosis.

3. Working diagram

The block diagram of RIGEL, including the typical pulse shapes at the different stages of the circuit, is shown in Fig. 2. The circuit has two steps, implemented in two different boards: first one master board (MS), and then a four output channels board (CH).

The aim of the master is to provide the channels with an array of reference ECL signals in order that they build the output pulses. For that purpose, the MS uses a high-frequency TTL waveform generator (MAX038), which allows frequency control by an external reference voltage. The output signal is differentiated

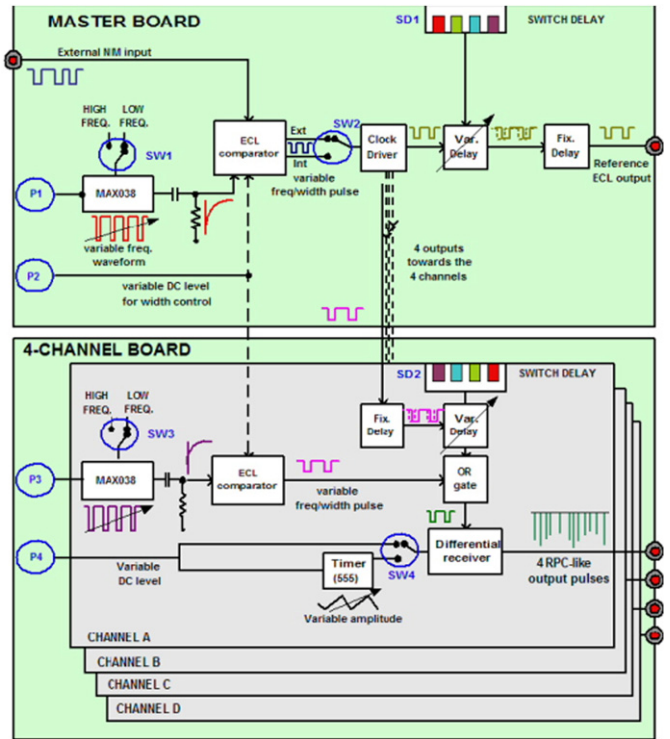


Fig. 2. Block diagram of RIGEL. Pulses patterns are depicted in the main stages of the circuit.

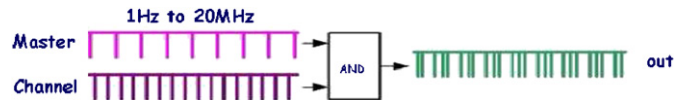


Fig. 3. The AND logic operation performed with the master timing signal on each channel allows the generation of random-like signals covering all inter-pulse delays.

and then compared with a reference voltage via the MC10E1651 dual ECL comparator. The reference voltage allows the control of the width of the output ECL pulses.

Optionally, the internal timing clock can be bypassed to use an external NIM clock instead. In this case the NIM signal is translated into ECL to match the logic required by the channels.

Before going to the channels, the signal generated on the MS is sent to the MC100EP14, a differential ECL clock driver that works as a multiplexer to provide five identical differential signals: four of them are addressed to the four channels, and the remaining one goes out as *START* signal. A variable delay allows the user to shift the *START* output with respect to the outputs of all the channels.

The circuitry on each channel is also based on the MAX038 and is implemented in the same way as in the master, and with the same tuning capabilities. In each channel, a new timing signal is generated and converted into ECL. This signal is combined with the master reference signal through an AND logic gate (Fig. 3). A variable delay allows shifting both signals, giving rise to adjustable and almost random patterns of pulses.

In each channel, a LM555 timer is used to generate a saw tooth wave, regulated in amplitude by a simple resistor divider. This wave is used to modulate the pulses pattern through a MC100EP16 ECL differential receiver/driver (Fig. 4). The output of the channel is an array of pulses, showing a random-like time distribution, with adjustable widths, rates and maximum amplitudes.

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