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Design and evaluation of a low-level RF control system analog/digital receiver for the ILC main LINACs

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ABSTRACT

The proposed RF distribution scheme for the two 15 km long ILC LINACs uses one klystron to feed 26 superconducting RF cavities operating at 1.3 GHz. For a precise control of the vector sum of the signals coming from the SC cavities, the control system needs a high-performance, low-cost, reliable and modular multichannel receiver. At Fermilab we developed a 96-channel, 1.3 GHz analog/digital receiver for the ILC LINAC LLRF control system. In this paper we present a balanced design approach to the specifications of each receiver section, the design choices made to fulfill the goals and a description of the prototyped system. The design is tested by measuring standard performance parameters, such as noise figure, linearity and temperature sensitivity. Measurements show that the design meets the specifications and it is comparable to other similar systems developed at other laboratories, in terms of performance.

1. Introduction

The proposed international linear collider (ILC) will be an electron/positron collider operating at 500 GeV (possible upgrade to 1 TeV) and will be composed of two damping rings, electron/positron source, detectors and two LINACs. The study in this paper applies also to other ILC-style LINACs, where one klystron drives multiple superconducting (SC) cavities. As presented in the reference design report for the ILC (RDR) [1], the RF distribution for the LINACs foresees 560 RF units, each of them composed of one klystron driving 26 SC cavities. They are located in three cryomodules in groups of nine, eight and nine cavities, respectively. The RF power from the klystron is distributed among the cavities through a series of hybrids, each with appropriate fractional coupling ($\frac{1}{9}$, $\frac{1}{8}$, ..., $\frac{1}{2}$) to get the same power at all cavities. The low power section of the RF system, also denoted as the low-level RF (LLRF), takes care of the control of the vector sum of signals coming from the SC cavities. The LLRF stabilizes the amplitude and phase of the vector sum at the desired set point by means of feedback and feedforward regulation techniques. In order to calculate the correction that is applied to the klystron, the LLRF control uses 96 RF signals coming from one RF station (26 cavities). The 96 RF channels is the sum of 26 field pick-up probes, 26 forward and 26 reflected wave signals, 3 phase references, 3 beam detectors, and the rest are for waveguide monitoring and spares. As a result, for the two LINACs, the overall sum of the RF signals that are processed by the multichannel receiver system equals 50,000. The high channel count has a major impact on the design of the LLRF receiver section, where all the incoming signals need to be downconverted and digitized. The process of downconversion and digitalization suffers from noise, nonlinearities, and temperature-dependent processes. In this paper we present the design strategies to address these problems and we exploit these strategies to implement a possible solution for the multichannel analog/digital receiver for an ILC style LINAC LLRF control system.

2. Requirements

The two main parameters that have the biggest impact on the design of the receiver are the performance and the high number of channels. In the RDR, the performance requirements are given in terms of controlled amplitude and phase of the RF fields, and they are derived from the requirements for luminosity of the collider. These numbers equal to 0.5% and 0.24° for correlated errors (e.g. ground motion, reference line drifts, beam loading, etc.) and 1.6% and 0.48° for uncorrelated errors (e.g. noise in one channel of the receiver). The errors are partitioned among the reference system (drifts of the reference line between RF stations), the perturbation sources of the cavity (microphonics, Lorentz force detuning and beam loading) and the LLRF electronics. The error

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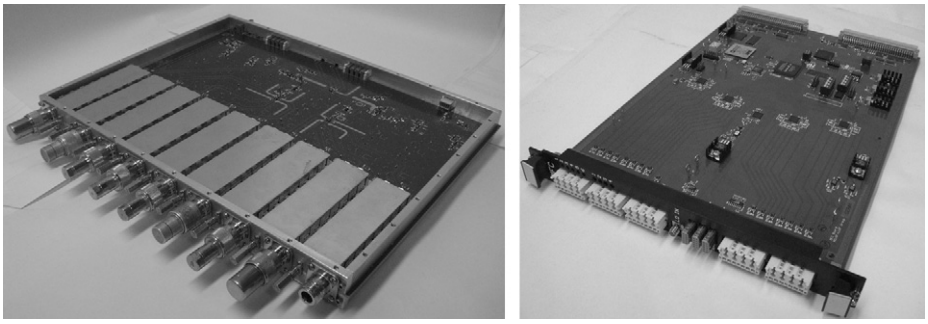

Fig. 1. The two printed circuit boards are the eight-channel analog receiver board [6] (on the left) and the 33-channel digital board [7] (on the right) also referred as the multichannel field controller module (MFC).

from the LLRF electronics is mainly defined by the errors from the receiver and the error from the LO generation/distribution [2,3]. The uncorrelated error introduced by one channel of the receiver (with the LO generation and distribution) that we aim for must be at least 20 times lower than the overall uncorrelated errors given in the RDR. This equals to 0.08% RMS and 0.024° RMS for amplitude and phase, respectively. Other disturbances like harmonics generated by the nonlinear electronics, coupling among adjacent channels and temperature-dependent drifts also have considerable effects on the system performance. However, they are not explicitly given in the RDR. In order to define some values for these parameters, as our design goals, we followed the philosophy that they must be limited by the most expensive part in the receiver chain, which is the analog-to-digital converter (ADC). We therefore aim for an isolation among channels that is higher than 90 dB and the second and third harmonics generated by the receiver must not exceed −75 dBc. Furthermore, we demand that the change of the amplitude and phase over large temperature swings (15 °C) meets uncorrelated amplitude and phase error values given above. We also expect that the resolution of the ADC will define the uncorrelated noise spectral density (NSD) of the receiver system at the output.

In addition to performance, the design has to account for the high number of RF channels that need to be processed. Due to the higher probability of failure, the high number of channels calls for a robust design to fit mean time between failure (MTBF) requirements and a modular design to minimize the mean time to repair (MTTR). In order to minimize MTBF we need to minimize the number of components in the system, which also means we aim for a simpler and lower cost design. Modularity can be achieved by properly grouping processing sections of the system which will eventually result in a more versatile design, with the possibility to be reused on other RF systems. The system with high number of channels also demands a high degree of automation, which would otherwise be impossible to calibrate, reprogram or diagnose in a short time period. Finally, the high channel count requires a cost- and power-sensitive design. The power consumption of the LLRF electronics that we aim for is less than 200 W per one RF station (96 channels).

3. System design strategy

The first step towards meeting the requirements for good performance, versatility and ease of automation is achieved by choosing the digital approach to system design. The commonly adopted digital architecture used in modern LLRF systems [4,5] is based on the software-defined radio (SDR) design, developed for the telecommunication market. The SDR philosophy is to digitize the signal as close to the antenna (cavity pick-up probe) as possible. This reduces the number of components, simplifies calibration of multiple channels and increases flexibility in digital signal processing. The typical SDR architecture uses direct sampling of RF signals with no downconversion to intermediate frequencies (IF). However, direct sampling degrades the signal-to-noise (SNR) ratio of the system due to the clock and aperture jitter of the ADC and digital-to-analog converter (DAC). For this reason, we chose instead to use the heterodyne approach, where the input RF signal at 1.3 GHz is downconverted to an IF at 13 MHz and then digitized.

The other important decision that has a major impact on modularity and cost is to use high channel density boards. This minimizes the number of boards needed per one RF station, decreases the group delay, simplifies the interconnections between the boards and reduces the possibility of failure. However, this decision also increases the number of traces and parts on the printed circuit board (PCB) close to the ADC. This eventually degrades signal integrity and makes the layout more complex. An additional problem associated with the high number of channels is finding an RF connector with satisfying isolation between channels that is compact and has acceptable return loss at 1.3 GHz. Many of the high-density and compact connectors we tested showed very poor isolation (>−50 dB) and return loss performances (>−15 dB) at 1.3 GHz. For this reason we decided to split the analog and the digital processing into two boards (see Fig. 1) and use the eight-channel coaxial connector (Harting, mini-coax) to interconnect the two boards.

3.1. Digital board design

In order to implement a high channel density board and at the same time solve the problem with the layout and signal integrity, extensive research has been done on various types of ADCs that the market is offering. The octal ADC (Analog Devices Inc., AD9222) with serial low-voltage differential signal (LVDS) output lines is a very convenient solution to this problem. It integrates eight channels on one chip and has only two (differential pair) output lines per ADC channel.

As mentioned in the introduction, we expect the NSD at the output of the receiver system to be equal to the NSD of the ADC, which was measured to be −147 dBc/Hz. Even though this noise level already satisfies the requirements for uncorrelated amplitude and phase errors given in the introduction, the expectations are even more optimistic. If we assume that the noise is uncorrelated, the vector sum will improve the SNR at the output of the ADC by app. 14 dB. It is worth noting that the relatively high ADC aperture jitter (800 fs) has little effect on the output NSD when the IF frequency is less than 50 MHz. For an IF of 13 MHz, the NSD (normalized to the carrier power) due to the aperture jitter equals −160 dBc/Hz, which is calculated using equations given by Kobayashi [8].