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# Fabrication of back-illuminated, fully depleted charge-coupled devices

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**Abstract**

We describe a fabrication strategy to produce fully depleted, back-illuminated charge-coupled devices (CCDs). Wafers are partially processed at a commercial foundry using standard processing techniques. The wafers are then thinned to the final desired thickness, and the processing steps necessary to produce back-illuminated devices are performed in our laboratory. The CCDs are then probed at wafer level, and we describe our techniques to screen for gate insulator flaws as well as defects on the back side of the wafer that are important for fully depleted devices.


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*Keywords:* Charge-coupled device; Fully depleted; High-resistivity silicon; Back illuminated; Fabrication techniques

## 1. Introduction

Large format, scientific charge-coupled devices (CCDs) are the detector of choice for imaging and spectroscopy at UV and visible wavelengths for ground- and space-based astronomy. For wide-field imaging it is necessary to have a large focal plane consisting of arrays of scientific CCDs. As an example of an existing camera, the MegaCam imager at the Canada–France–Hawaii Telescope consists of 40, $2048 \times 4162$ (13.5 μm pixel) CCDs [1]. Larger focal plane arrays are proposed, including the Subaru Telescope HyperSuprime camera with plans for 176, $2048 \times 4096$ (15 μm pixel) CCDs [2], and the Large Synoptic Survey Telescope camera where approximately 200 imagers are required [3].

In order to achieve this major increase in pixel counts, it is necessary to develop robust CCD fabrication methods that result in high yield. Cost is a consideration given that the present-day price of scientific CCDs is approximately \$50–100k per $2k \times 4k$ CCD.

In this work we describe fabrication techniques used at the Lawrence Berkeley National Laboratory (LBNL) to fabricate scientific CCDs. The CCDs developed at LBNL are fabricated on high-resistivity silicon, and as a result, relatively thick, fully depleted devices are realized [4]. We have demonstrated that the processing necessary to produce back-illuminated CCDs can be done at the wafer level and in batches of multiple wafers. This allows for high throughput and good repeatability since the processing steps are done nearly simultaneously for the batch.

## 2. Fully depleted CCD operating principles and fabrication

Fig. 1(a) shows a cross-sectional drawing generated from the process simulation program TSUPREM4 [5] of the fully depleted, back-illuminated CCD described in this work. The CCD thickness, typically 200–300 μm, results in improved near-infrared response when compared to standard scientific CCDs that are thinned to 20 μm thickness and below. The CCDs are fully depleted by the use of a substrate bias voltage. This results in a spatial resolution that can be controlled via CCD thickness, substrate bias voltage, and operating temperature.

Fig. 1(b) shows a simplified cross-section and an equivalent circuit. Since the substrate capacitance $C_{sub} = \varepsilon_{Si}/y_N$ for a thick device is much less than $C_{eq}$, the series combination of the p channel and gate insulator capacitance, the substrate bias voltage has little effect on the potential in the CCD channel. $y_N$ is the substrate thickness

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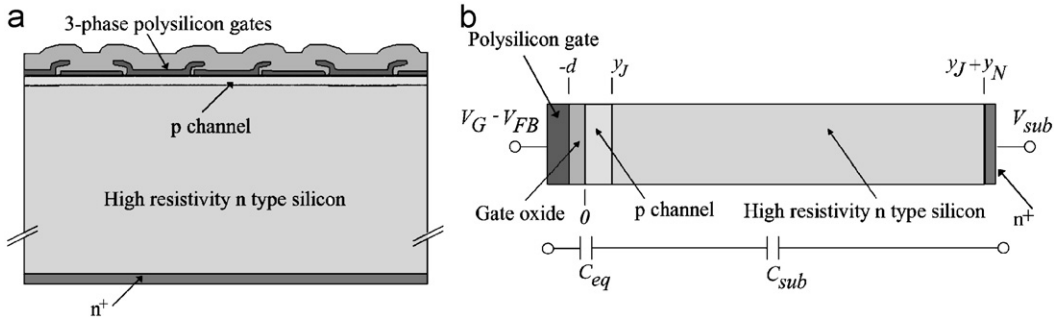


Fig. 1. (a) Cross-sectional drawing of the CCD described in this work. The cross-section was generated by the process simulator TSUPREM4 [5]. (b) Simplified cross-section and the equivalent circuit.

and $\varepsilon_{Si}$ is the permittivity of silicon. Therefore this type of CCD can be operated over a wide range of substrate bias voltages, and we have demonstrated operation of both 200 and 650 μm thick CCDs at voltages as high as 200 V [6].

The buried-channel, three-phase CCD is fabricated in a 150 mm wafer, triple-polysilicon process with a minimum feature size of 2.5 μm. Most of the fabrication is done at a commercial foundry (DALSA Semiconductor). The advantages of working with a commercial foundry include fast turnaround, good repeatability from run to run, access to a large number of process steps, and economies of scale.

However, fabrication of back-illuminated CCDs requires deviations from typical silicon processing. Science requirements often dictate a wafer thickness that is not the same as the standard wafer thickness used in the foundry. For example, spatial resolution requirements for the SuperNova Acceleration Probe [7] require a wafer thickness of approximately 200 μm, which is to be compared to the standard 150 mm wafer thickness of 675 μm. Such a wide range of thickness usually exceeds the limits over which standard photolithography equipment can achieve proper focus. Also, in our experience 200 μm thick, 150 mm wafers are fairly robust to breakage, but some care is required in wafer handling. Because of these considerations we have found it necessary to develop in-house the technologies necessary to produce fully depleted, back-illuminated CCDs.

The fabrication work at LBNL is done at the Micro-Systems Laboratory (MSL), a Class 10 clean room. The wafers are processed through 8 of the 11 photomasking steps at DALSA Semiconductor. A small number of wafers are then completed at DALSA Semiconductor for quality control purposes, with the remaining wafers sent to our laboratory. The latter are then sent to a commercial vendor where they are thinned to the desired final thickness. In addition to thinning, the wafer back sides are polished to a prime wafer finish at this step. Since the thinned wafers will go through photolithography steps, it is a requirement that the wafers be sufficiently flat after the thinning process. We typically achieve a total thickness variation of 8 μm or better after thinning, which is compatible with the 12 μm depth of focus for the projection aligner used at LBNL.

After thinning, the wafers are returned to LBNL and a thin in situ doped polysilicon (ISDP) layer is deposited to form the back side $n^+$ contact shown in Fig. 1. This layer must be thin for good blue and UV response and also must be able to tolerate full depletion without an increase in dark current. The typical thickness is 20–25 nm. This layer is deposited by low-pressure, chemical-vapor deposition at 650 °C in a horizontal reactor furnace.

The thin ISDP layer is then removed from the front surface of the wafer by plasma etching and the first lithography step is performed on the thinned wafers. In order to match the lithography equipment at the commercial foundry, alignment verniers are included at four locations on the wafer. Layer to layer registration measurements are taken on the verniers, and alignment errors including translation, magnification, and skew can be corrected. Once this is done the alignment errors are typically smaller than 0.5 μm.

The remainder of the processing includes contact and metal photolithography and etching, alloying of contacts, and deposition of back side anti-reflection coatings by radio-frequency sputtering.

We have found that plasma etching of the contact openings in $SiO_2$ is one of the more difficult steps in the process. CCDs have large gate electrode areas and are susceptible to plasma damage. We have utilized commercially available plasma monitor wafers to assist in the development of low-damage etch processes [8].

## 3. Unique fabrication issues for fully depleted, back-illuminated CCDs

Once the ISDP layer is deposited the back surfaces of the wafers will come into contact with automated wafer handling equipment. We have observed that particles and residue from the various vacuum chucks and wafer handlers can imprint patterns onto the back surface of the CCD. Fig. 2(a) shows a contrast-enhanced image taken with a $3512^2$, 10.5 μm pixel CCD that was uniformly illuminated at an ultraviolet wavelength of 350 nm. Weak patterns from wafer handling equipment are visible. At this illumination wavelength the absorption depth is small,