

DEPFET, a monolithic active pixel sensor for the ILC[☆]

J.J. Velthuis^{a,*}, R. Kohrs^a, M. Mathes^a, A. Raspereza^e, L. Reuen^a, L. Andricek^c, M. Koch^a,
Z. Dolezal^d, P. Fischer^b, A. Frey^e, F. Giesen^b, P. Kodys^d, C. Kreidl^b, H. Krüger^a,
P. Lodomez^a, G. Lutz^c, H.G. Moser^c, R.H. Richter^c, C. Sandow^a, D. Scheirich^d,
E. von Törne^a, M. Trimpl^a, Q. Wei^c, N. Wermes^a

^aUniversity of Bonn, Physikalisches Institut, Nussallee 12, D-53115 Bonn, Germany

^bUniversity of Mannheim, B6 26, D-68161 Mannheim, Germany

^cMax Planck Institute Semiconductor Laboratory, Otto-Hahn-Ring 6, D-81739 München, Germany

^dCharles University, Institute of Particle and Nuclear Physics, V. Holesovickach 2, CZ-18000 Praha, Czech Republic

^eMax-Planck-Institut für Physik, Föhringer Ring 6, D-80805 München, Germany

Available online 26 May 2007

Abstract

In a DEPLETED Field Effect Transistor (DEPFET) sensor a MOSFET is integrated on a sidewards depleted p-on-n silicon detector, thereby combining the advantages of a fully depleted silicon sensor with in-pixel amplification. A 450 μm thick DEPFET was tested in a testbeam. The S/N was found to be larger than 110. The position resolution is better than 5 μm . At a seed cut of 7σ , the efficiency and purity are both close to 100%. In the readout chip a zero-suppression capability is implemented. The functionality was demonstrated using a radio-active source. The predicted impact parameter resolution of a 50 μm thick DEPFET vertex detector, is much better than required for the International Linear Collider (ILC).

© 2007 Elsevier B.V. All rights reserved.

PACS: 29.90.W; 29.40.G; 42.79.P

Keywords: Active pixel sensors; CMOS; Tracking; Solid state detectors

1. Introduction

For the accurate measurement of Higgs branching ratios and properties as well as precise studies of physics processes beyond the Standard Model at the International Linear Collider (ILC), efficient distinction of heavy quark flavors, most notably of bottom and charm quarks, is a must. This requires precise secondary and even tertiary vertex detection, correct assignment of every track to the correct vertex and determination of the jet charge.

Since the impact parameter of b-quarks is in the order of $\sim 300 \mu\text{m}$ and of c-quarks $\sim 100 \mu\text{m}$, the challenge for a vertex detector at the ILC is to build a very low mass, high

precision vertex detector. The aims are a single hit resolution better than 5 μm and a radiation length less than 0.1% X_0 for a ladder, which requires $\sim 50 \mu\text{m}$ thick silicon sensors. The very low mass requirement implicates that no active cooling can be used. Therefore, the detectors power consumption is limited to amounts that can be removed by flowing gas through the detector.

Due to the very high beamstrahlung rate near the interaction point, which produces e^+e^- -pairs in vast numbers, the background conditions and the time structure of the accelerator are leading to detector occupancies of $\sim 100 \text{ hits}/\text{mm}^2/\text{bunch train}$ ($\sim 1 \text{ ms}$) for a pixel detector situated 15 mm away from the beam line [1].

Also the time structure of the ILC provides a challenge. There will be 2820 bunches per pulse, which are spaced 337 ns apart, leading to a pulse train of 950 μs which has a repetition rate of 5 Hz. The aim is to readout the sensors 20 times during a bunch train. In our current design this

[☆]This work was supported by the Alexander von Humboldt Foundation, Germany.

*Corresponding author. Tel.: +49228733608.

E-mail address: velthuis@physik.uni-bonn.de (J.J. Velthuis).

requires a row readout rate of 20 MHz. To limit the power consumption the readout chips need to be switched off in between the bunch trains. The radiation load is modest. The detector has to withstand 200 krad for 5 years operation [2].

The DEPLETED Field Effect Transistor structure, abbreviated DEPFET [3], provides detection and amplification properties together. The principle of operation is shown in Fig. 1. A MOS or junction field effect transistor is integrated onto a detector substrate. By means of side-wards depletion, appropriate bulk, source and drain potentials, and an additional deep-n-implantation, a potential minimum for electrons is created right underneath the transistor channel ($\sim 1 \mu\text{m}$ below the surface). This can be regarded as an internal gate of the transistor. A particle entering the detector creates electron–hole pairs in the fully depleted silicon substrate. While the holes drift to the rear contact of the detector, the electrons are collected in the internal gate where they are kept stored. The signal charge leads to a change in the potential of the internal gate, resulting in a modulation of the channel current of the

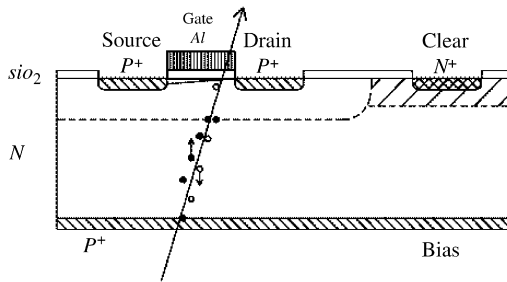


Fig. 1. DEPFET principle.

transistor. The signal charges are cleared out of the internal gate by a positive voltage at the CLEAR contact. Note that the signal is not destroyed by the readout until the clear pulse is issued, hence allowing multiple readout.

The low noise is obtained because of the small capacitance of the internal gate (several 10 fF) and the absence of external connections to the first amplification stage. The high signal is due to the charge collection in a fully depleted bulk. Both together yield a very large S/N

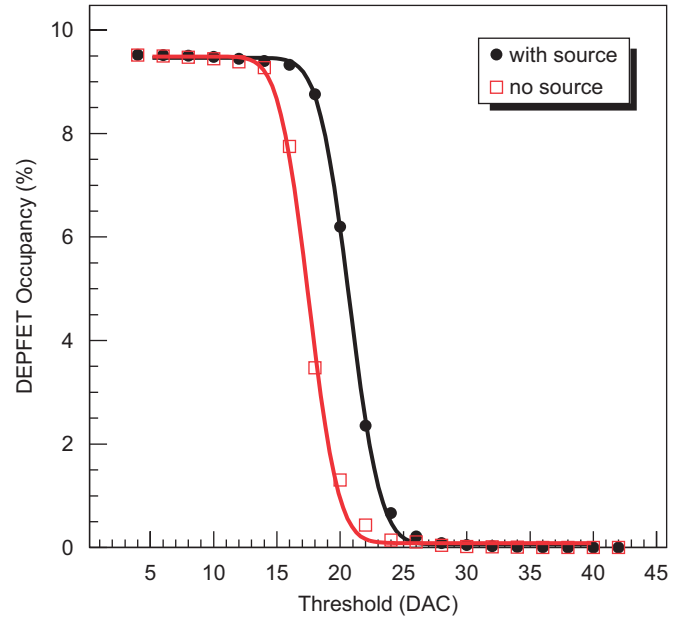


Fig. 3. Entire DEPFET occupancy as a function of the threshold with and without a radio-active source, demonstrating that the zero-suppression works. Note that the occupancy is limited by the buffer size.

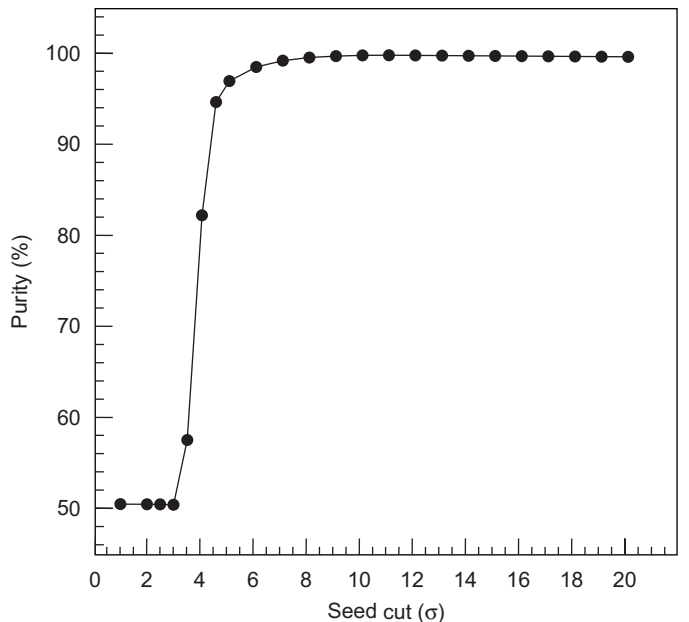
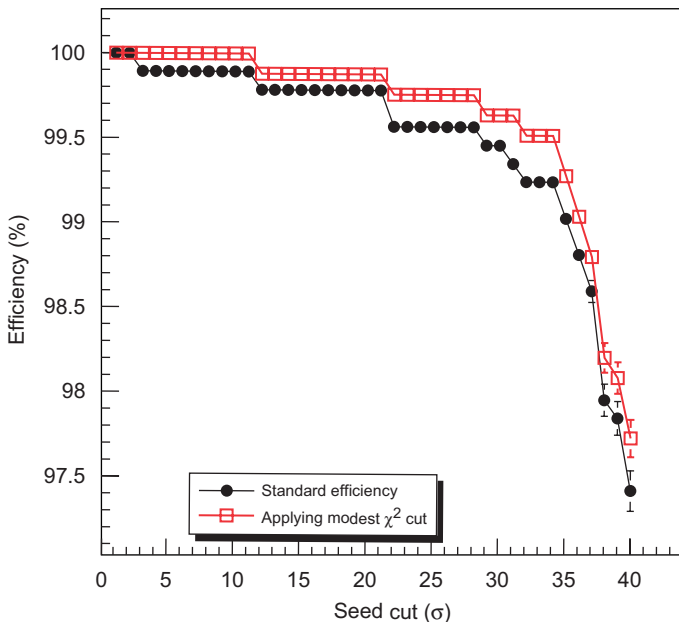


Fig. 2. Efficiency and purity as a function of the seed cut.

Download English Version:

<https://daneshyari.com/en/article/1830043>

Download Persian Version:

<https://daneshyari.com/article/1830043>

[Daneshyari.com](https://daneshyari.com)