Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 579 (2007) 750–753
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

SiLC R&D: Design, present status and perspectives

M. Lozano[a], R. Orava[b], N. van Remortel[b], M. Frey[c], F. Hartmann[c], Th. Müller[c], V. Saveliev[d], Z. Doležal[e,*], Z. Drásal[e], P. Kodyš[e], P. Kvasnička[e], D. Scheirich[e], Ph. Bailly[f], M. Berggren[f], G. Daubard[f], J. David[f], M. Dhellot[f], J.F. Genat[f], T.H. Hung[f], J.F. Huppert[f], D. Imbault[f], F. Kapusta[f], H. Lebollo[f], Ph. Repain[f], F. Rossel[f], A. Savoy-Navarro[f], W. Da Silva[f], M. Fernandez[g], C. Martinez Rivero[g], A. Ruiz[g], I. Vila[g], J. Fuster[h], C. Lacasta Llacer[h], P. Modesto[h], Th. Bergauer[i], M. Krammer[i]

[a]*Centro Nacional de Microelectronica, IMB-CNM/CSIC, Barcelona, Spain*
[b]*Department of Physical Sciences, University of Helsinki and Helsinki Institute of Physics, Helsinki, Finland*
[c]*Institut für Experimentelle Kernphysik, Karlsruhe University, Germany*
[d]*Department of Applied Mathematics, Obninsk State University of Atomic Energy, Obninsk, Russia*
[e]*Faculty of Mathematics and Physics, Charles University, V Holešovičkách 2, Prague, The Czech Republic*
[f]*Laboratoire de Physique Nucleaire et des Hautes Energies, Universites Paris 6 et 7/CNRS-IN2P3, France*
[g]*Instituto de Fisica de Cantabria (CSIC-Cantabria University), Santander, Spain*
[h]*Instituto de Fisica Corpuscular (IFIC), Universidad de Valencia, CSIC, Valencia, Spain*
[i]*Institute of High Energy Physics, Austrian Academy of Science, Vienna, Austria*

Available online 31 May 2007

Abstract

This paper briefly describes the main R&D objectives that are undertaken within the international R&D collaboration SiLC aiming to build the next generation of silicon tracking devices especially in the case of the ILC. Firstly, motivation to use silicon detectors in the tracker is explained. Then basic aspects of the design and solutions proposed are described (sensors, front-end electronics, mechanics, alignment). First results from the lab and beam test of the front-end chips and module prototypes built are shown.

PACS: 29.40.Gx; 29.40.Wk

Keywords: Tracking; Position-sensitive detectors; Strip detectors; International Linear Collider

1. Introduction

Over the last decade, a consensus has emerged in the community of particle physicists that a high-luminosity high-energy electron–positron collider (now known as ILC-International Linear Collider) is an essential step on the road of understanding electroweak symmetry breaking and finding the particles which account for dark matter.

The enormous statistical power of the ILC machine and the favourable background conditions should be matched by a precision detector which is capable of taking collision data with the least possible introduction of biases and systematic errors. The required resolutions are challenging for most of the subsystems. Currently, several overall detector concepts are studied. The main differences are in the choices for charged particle tracking and in the magnetic field and inner radius of the electromagnetic calorimeter. The SiD [1] concept employs a 5 T magnetic field and an all-silicon tracking system. The LDC [2] concept has a 4 T field and relies on a large time projection chamber (TPC) supplemented by few layers of silicon detectors for tracking. In the GLD [3] concept a 3 T magnetic field is compensated by an even larger calorimeter radius. While both in SiD and LDC a silicon–tungsten electromagnetic calorimeter (ECAL) with 1 cm^2 cells is

*Corresponding author. Tel.: +420 221 912 456; fax: +420 221 912 434.
E-mail address: Zdenek.Dolezal@mff.cuni.cz (Z. Doležal).

0168-9002/$ - see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2007.05.286

foreseen, GLD relies on a scintillator—tungsten ECAL with crossed 14 cm^2 scintillator tiles. Recently, 4th concept [4] was presented differing namely in calorimetry and muon system.

The requirements for charged particle tracking are mainly high efficiency, robustness, and good double track resolution. However, for some important physics channels very high-momentum resolution ($\sigma(1/p_t) = 5 \times 10^{-5}\,GeV^{-1}$) has to be achieved, approximately a factor five better than achieved at LEP. The current ideas are described in the following sections.

2. Silicon tracking at ILC

Two complementary approaches to achieve these requirements on the ILC detector tracker are being pursued: silicon strip detectors which give a small (≈ 5) number of very precise (few micrometers) space points or a huge TPC with at least 200 space points of moderate ($<100\,\mu m$) point resolution. In the case of silicon tracking the major challenges are to achieve the desired point resolution with a minimum of material to reduce multiple scattering and photon conversions.

In the existing detector concepts various options are proposed: the SiD concept intends to use purely silicon as a sensor technology for most sub-detector systems. The SiLC collaboration [5] has proposed for the detector concepts that have a TPC for central tracking (i.e. LDC and GLD concepts) to complete this tracking system with a system of Silicon trackers that is called the "Silicon envelope" [6]. It consists of silicon sensors in the endcap region (ECT), in the innermost central (SIT) and forward (FCH) parts and in between the TPC and the central e.m. calorimeter (SET).

Silicon layers surrounding a TPC could provide for improved momentum resolution, improved interfacing to the calorimeter and vertex detector, and act as a robust fiducial for the calibration of the TPC (see Fig. 1). On the other hand, current all-silicon tracking designs are expected to exhibit a precision fully competitive with that of gaseous tracking options, while offering the potential for a substantial savings in material (particularly in the forward direction), a more straight-forward calibration procedure, and greater resistance to backgrounds and aging.

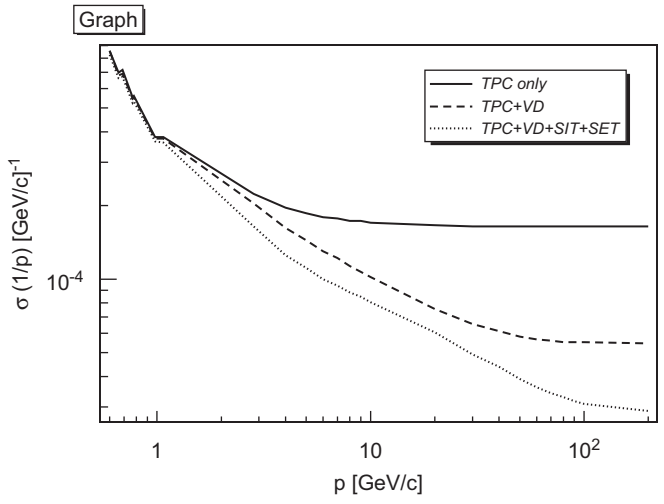

Fig. 1. Effect of supplementary silicon tracking on the momentum resolution. TPC: Time Projection Chamber, VD: Vertex Detector, SIT, SET: Silicon Internal and External Tracker, respectively.

3. Sensors

The SiLC concept of a silicon tracker utilizes state-of-the-art technologies in all aspects of the design. For the sensor, the baseline consists of microstrip detectors, built from larger size wafers (wafer diameter at least 8 in.), both single and double-sided, and thinned by a factor of 2 or 3. The thickness of sensors planned for ILC is a topic for study. New pixel technology might also be of interest, in particular for the second layer near the vertex detector in the central inner part. Currently, similar sensors fabricated for Glast and CMS are being used for module prototyping. Design and production of dedicated SiLC sensors is planned for 2007.

4. Electronics

The readout electronic system should not degrade significantly the intrinsic detector performance within the environment of the ILC detectors, matching therefore several constraints: be compatible with the duty cycle of the ILC machine, ensure a signal to noise ratio of 25 at 3 μs shaping time for MIPs; provide a continuous stream of lossless compressed digital data at the end of each bunch train. At the same time the electronics should dissipate a total average power under 15 W (with 1:100 duty cycle), minimize the on-detector total material regarding transparency to radiation and ensure the reliability of the whole system.

The general architecture of the front-end chip (see Fig. 2) is based on a low-noise preamplifier, a pulse shaper, a zero suppression decision, a sampling analog pipe-line, an analog to digital converter, a digital buffer, an internal calibration, and power switching circuitry for power cycling. Two ranges of shaping times are implemented, namely a "slow" shaping time between from 500 ns and a few μs, and a "fast" shaping time focusing on a few tenths of ns, in order to obtain a rough measurement of the z coordinate along the beam axis. This fast shaping time could also be used to provide a fine BCO (Bunch Crossing Over) tagging in case of high occupancy in some regions.

As one of the first results of the SiLC R&D program, a test chip SiTR-180 in 180 nm CMOS technology has been designed and tested. Results have been encouraging concerning the main specifications such as noise and power. The power consumption of preamplifier and shaper is 0.3 mW/channel, so power dissipation below 1 mW/channel (without power cycling) for the whole system of the front-end chain described above is achievable [7]. The preamplifier gain of the chip is around 8 mV/MIP with