Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 579 (2007) 769–774
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

Total dose dependence of oxide charge, interstrip capacitance and breakdown behavior of sLHC prototype silicon strip detectors and test structures of the SMART collaboration

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Available online 29 May 2007

Abstract

Within the R&D Program for the luminosity upgrade proposed for the Large Hadron Collider (LHC), silicon strip detectors (SSD) and test structures (TS) were manufactured on several high-resistivity substrates: p-type Magnetic Czochralski (MCz) and Float Zone (FZ), and n-type FZ. To test total dose (TID) effects they were irradiated with ^{60}Co gammas and the impact of surface radiation damage on the detector properties was studied. Selected results from the pre-rad and post-rad characterization of detectors and TS are presented, in particular interstrip capacitance and resistance, break-down voltage, flatband voltage and oxide charge. Surface damage effects show saturation after 150 krad and breakdown performance improves considerably after 210 krad. Annealing was performed both at room temperature and at 60 °C, and large effects on the surface parameters observed.

PACS: 29.40.Gx; 29.40.Wk; 61.80.Ed; 61.82.Fk; 84.37.+q; 85.30.De

Keywords: Solid-state detectors; Position sensitive detectors; Radiation effects on semiconductors; Gamma ray effects; Electrical variable measurements; Semiconductor device characterization

1. Motivation

The future luminosity upgrade proposed for the Large Hadron Collider (LHC), the Super-LHC (sLHC), requires a critical evaluation of the radiation hardness of the silicon strip detectors (SSD) proposed as main tracking detectors in the Inner Detector (ID) of the upgraded LHC detectors [1]. The CERN R&D collaboration RD50 was formed to investigate radiation damage in semiconductor detectors and develop radiation-tolerant tracking detectors [2]. The INFN funded SMART project that involves several Italian institutes belonging to RD50, has fabricated SSDs and test structures (TS) on various high-resistivity substrates [3]. The aim of this activity is to thoroughly characterize the different design/technology options so as to understand the details of fabrication steps which will permit the fabrication of radiation-tolerant SSDs.

As far as bulk radiation damage is concerned, which is the main problem to face since it reduces the collected charge, promising results have already been reported [4]. However, surface damage effects should also be consid-

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doi:10.1016/j.nima.2007.05.287

ered, since they might influence the noise performance. This is especially relevant for detectors built on p-type substrates, for which isolation structures (p-stop or p-spray) are needed in between the n^+ strips to interrupt the inversion electron layer induced by the positive fixed oxide charge. In fact, simulation studies have clearly evidenced the strong impact of surface effects (oxide charge, surface states) on the interstrip capacitance and the breakdown voltage, as well as on the isolation properties of the p-stop/p-spray regions [5]. This paper describes experimental results from the electrical characterization of strip detectors and TS irradiated with ^{60}Co to test total dose effects. The TID levels for the sLHC, mainly due to charged particles, are expected to exceed 100 Mrad close to the collision region, while effects at the $Si–SiO_2$ interface have been shown to saturate typically at the 100 krad level [6].

Table 1
Structures investigated

Type	Dimension	Measurements	Frequency
MOS capacitor	Circular area = 3.14 mm^2	C–V	10 kHz
Capacitance TS	Length = 1.15 cm	C_{int}–V	~1 MHz
	Pitch = 50, 100 μm	C–V	10 kHz
	Implant = 15, 25 μm	I–V	n.a.
	Poly width = 10 μm		
	Metal = 23, 33 μm		
SSD	Length = 4.46 cm	C_{int}–V	~1 MHz
	Pitch = 50, 100 μm	C–V	10 kHz
	Implant = various	I–V	n.a.

Table 2
Wafers investigated

Wafer type	Wafer #	Thickness (μm)	p-spray dose (cm^{-2})	SSD/TS/MOS
n FZ	W1254	300	n.a.	TS, MOS
p FZ	W084	200	5×10^{12}	TS, MOS
p FZ	W014	200	3×10^{12}	SSD
p FZ	W037	200	5×10^{12}	SSD
p MCz	W044	300	3×10^{12}, no passivation	TS, MOS
p MCz	W253	300	5×10^{12}, no passivation	TS, MOS
p MCz	W066	300	3×10^{12}, no passivation	SSD
p MCz	W182	300	5×10^{12}, no passivation	SSD

2. Devices

A set of TS and SSDs were fabricated on several different wafer types at ITC-irst in Trento, Italy. They include, as shown in Table 1 for this study, short SSD of varying strip width and pitch, circular MOS capacitors with aluminum top electrode, and capacitance TS, which are mini strip detectors. Results are presented for a subset of the available SMART wafers, as listed in Table 2. The n-type Float Zone (FZ) and the p-type Magnetic Czochralski (MCz) were 300 μm thick, while the p-type FZ had a thickness of 200 μm. The p-type wafers were processed with two different p-spray doses to isolate the strips: 3×10^{12} cm^{-3} (“low p-spray dose”) and 5×10^{12} cm^{-3} (“high p-spray dose”). Table 3 lists the details of the SSD investigated.

3. Sample preparation

The TS are comprised of 9 AC coupled strips, of which the inner-most three allow the measurement of the interstrip capacitance from the central strip to its pair of next neighbors, and the outer three strips on each side are connected together to allow bonded connections to a shield, for which we used the bias ring. We compared the interstrip capacitance of a test structure with the one of a 4.45 cm long mini-SSD, where the interstrip capacitance was measured to 3 pairs of next neighbors, with the next 3 strips on each side grounded to shield. Results of these measurements are shown in Fig. 1. The expected ratio of 1.2 between the geometrical values of capacitance/length to the next pair and to the next three pairs is observed [7]. It should be noted that pre-rad one observes a large effect on the interstrip capacitance whether the shield strips are bonded to the bias ring or not. This difference disappears post-rad.

Table 3
p-type SSD investigated

SSD	Substrate	p-spray dose (cm^{-2})	Pitch (μm)	# strips	Implant width (μm)	Poly width (μm)	Metal width (μm)
14-5	FZ	3×10^{12}	50	64	15	10	27
14-8	FZ	3×10^{12}	100	32	35	30	43
37-5	FZ	5×10^{12}	50	64	15	10	27
37-8	FZ	5×10^{12}	100	32	35	30	43
66-8	MCz	3×10^{12}	100	32	35	30	43
182-5	MCz	5×10^{12}	50	64	15	10	27
182-8	MCz	5×10^{12}	100	32	35	30	43