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Operational experience of the CDF[1] Run II silicon detector

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Abstract

The CDF Run II silicon detector is a 722,432 channel system designed to perform precision tracking and vertex measurements. After a challenging commissioning period, this detector is now used in regular data taking, recording 1 fb^{-1} of data over the last four years. A summary of the problems encountered during commissioning is given as well as experiences of maintaining and operating such a large, complex detector. A comment on the longevity of the silicon detector is also given.

Keywords: Silicon vertex detector; CDF; Tevatron; Single-event upset; Radiation damage

1. CDF Run II silicon detector

The Run II silicon detector allows CDF [1] to perform precision tracking and measure displaced vertices. It is one of the largest operating silicon tracking detectors in high-energy physics. The detector has 7–8 layers with 722,432 channels spread over 704 ladders and 5644 read out chips. In total, the silicon sensors cover a surface area of approximately 6 m^2.

The CDF silicon detector is composed of three sub-detectors: Silicon Vertex Detector II (SVX-II), Intermediate Silicon Layer (ISL), and Layer Zero–Zero (L00) (see Fig. 1).

1.1. SVX-II

The core of the CDF Run II silicon detector is the SVX-II [2]. It is approximately 1 m long with five layers of silicon at radii from 2.5 cm to 10.6 cm. It is divided into three mechanical barrels along its length with electrical read out at either end. All the silicon sensors are double-sided sensors. Three of the five silicon layers have axial and 90° azimuthal strips while the remaining two have axial and small angle stereo strips at 1.2°. The strip pitch varies from 60 μm to 140 μm.

The five silicon layers are arranged in $r\varphi$ as twelve 30° wedges. Each wedge is read out in parallel.

1.2. Intermediate silicon layer (ISL)

The ISL [3] was added to extend the silicon tracking to high pseudorapidity[2] and to link tracks between the outer wire chamber and the SVX-II as part of an integrated tracking system. The ISL is composed of one central layer and two outer layers. The ISL layers use double-sided small angle (1.2°) stereo strips. The strip pitch for both sides is 112 μm.

1.3. Layer zero–zero (l00)

L00 [4] is a single layer of single-sided silicon strips mounted close to the beam pipe. This allows precision hit position measurements before scattering by the detector material. Therefore, the material budget was kept low; 0.6–1.0% of a radiation length. The strip pitch is 25 μm but only alternate strips are read out which allows good spatial resolution at low signal-to-noise ratio.

1.4. The SVX3D read out chip

All the silicon sensors are read out by the SVX3D chip [5], which is a 128 channel device. Each channel has an

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[1]CDF: Collider Detector at Fermilab.

[2]Pseudorapidity, $\eta = -\ln\tan(\theta/2)$ where θ is angle of the track with respect to the z-axis (proton direction).

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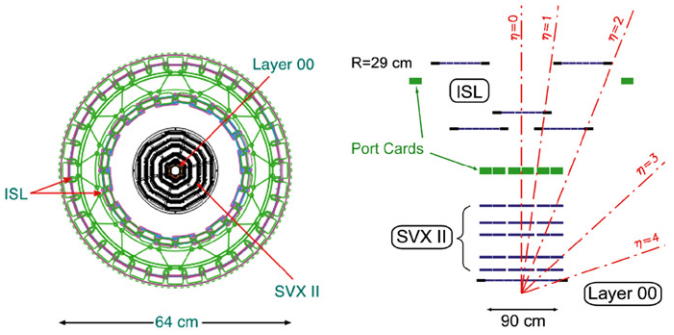

Fig. 1. Views of the CDF silicon detector. The projections of the sub-detectors in $r\varphi$ (left) and rz (right) are shown.

analog integrator, a 47 cell analogue pipeline and an 8 bit Wilkinson-type ADC. The chip also has the following features:

- *Deadtime-less operation*: It can acquire charge while digitisation of a previous sample is taking place.
- *Dynamic Pedestal Subtraction* (*DPS*): The chip subtracts any common-mode noise.
- *Sparsification*: Does not read out channels below a programmable threshold.
- It has a series of programmable settings to optimise the charge collection while minimising the current consumption.

The SVX3D chip was fabricated using the Honeywell CMOS 0.8 μm radiation hard process. Irradiations up to 4 Mrad with ^{60}Co sources and 15 Mrad with 55 MeV proton source have been carried out. The measurements show the chip noise in the innermost SVX layer would increase by 17% after 8 fb^{-1} (3.1 Mrad) [6].

The large number of chips in the system dissipates approximately 3 kW of power. Therefore, the entire detector needs to be actively cooled.

2. Silicon detector commissioning

The commissioning was lengthy and challenging in part due to the complexity of the system. Some of the ISL cooling lines were found to be blocked with epoxy. A laser was used to cut a hole through the epoxy. L00 had two problems. Firstly, the power supplies failed due to a radiation-soft component. So all supplies had to be replaced. Secondly, the pedestals across a L00 read out chip were not uniform [4]. It was discovered that L00 was suffering from pick-up along the long analogue leads connecting the sensors to the read out chips. This prevented the use of the SVX3D dynamic pedestal subtraction. The only solution was to read out the entire ladder and to perform a software pedestal subtraction.

2.1. Wirebond resonances

The most challenging of the commissioning problems were the *wirebond resonances* [7]. The wirebonds connecting the rφ and z sides of the silicon sensors would fail under anomalous trigger conditions. As these wirebonds are orthogonal to the 1.4 T magnetic field, any current fluctuations would induce a Lorentz force on the wires. During consecutive, *synchronous* chip read outs, this would drive the wires to resonance and cause them to break. 12 out of the 360 SVX ladders were damaged by these wirebond resonances.

The wirebond failures could have been prevented if the wirebonds were encapsulated. However, this was only discovered after the installation of the silicon detector. Instead, a hardware solution was developed to detect the onset of resonance conditions. Since the addition of this resonance protection board, no further ladders have suffered from wirebond resonance failures.

3. Silicon detector operations

Despite the difficulties during commissioning, the detector is operating well and is used routinely in data taking. Ninety-three percent of all ladders are powered and 84% are giving data with an error-rate $<1\%$. The measured signal-to-noise ratio is 10 for L00, 14(12) for SVX-II $r\varphi(z)$ sides and 12 for ISL.

The physics performance is measured using muons reconstructed by the wire chamber. The track finding efficiency is 94% if three $r\varphi$ layer hits are required and 90% for four layers [8].

However, maintaining the detector at this level of efficiency requires a lot of effort. At least two people are on 24 hour call. The current activities which occupy the group are beam incidents, single-event-upset class of failures and low light levels in the Dense Optical Interface Module (DOIM) [9] optical data link.

3.1. Beam incidents

Due to the proximity of the CDF silicon detector to the Tevatron beam line, it is particularly sensitive to any abnormal or unstable beam conditions. There are two types of incidents which are of concern to the silicon detector: quenches of the Tevatron superconducting magnets and the *kicker-prefire* (asynchronous beam abort). The magnet quenches have so far not been serious. On the other hand, *kicker-prefire* incidents have been far more damaging.

The *kicker-prefire* is a Tevatron term for an asynchronous beam abort. Under normal operating conditions, the kicker magnet safely disposes the beam. However, during a *prefire* the kicker system fires spontaneously to send fragments of the Tevatron beam to the CDF detector.

During these types of incidents, the SVX3D chips have been most affected. The large instantaneous dose of charge induces large currents in the read out chips; the currents are so large that the detector safety interlocks switch power off to the effected ladder. The effected chips become unresponsive. Unfortunately, due to the daisy-chain design,