Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 567 (2006) 184–187
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

The front-end electronics of the LHCb ring-imaging-Cherenkov system

K. Wyllie*

CERN, Geneva, Switzerland

On behalf of the LHCb RICH collaboration

Available online 23 June 2006

Abstract

The LHCb experiment at the CERN Large Hadron Collider will use ring-imaging Cherenkov detectors for particle identification. By measuring rings of Cherenkov photons generated by elementary particles traversing a radiative medium, these particles can be identified across a wide range of momenta. The photons will be measured by a new type of detector, the pixel hybrid photon detector (HPD). In total, 484 HPDs will be used, providing ~500,000 channels of data. Specific readout electronics have been developed for processing the data from the HPDs, and this paper describes the design and testing of these devices together with the final system to be used in the experiment. Emphasis is on the application-specific integrated circuits that are encapsulated within the HPDs, allowing high channel density and low noise. These are subject to the strict requirements of efficient photon detection and reliability within the harsh environment of the experiment. Special interconnect techniques developed for this application are described. Finally, the additional electronics infrastructure to readout the full system of 500,000 channels is outlined, including data transmission and power distribution.

PACS: 29.40.Ka; 29.40.Wk

Keywords: Hybrid photon detectors; Pixel detectors; CMOS; Flip-chip bonding

1. Introduction

The LHCb ring-imaging-Cherenkov (RICH) [1] system will use a novel type of detector, the pixel hybrid photon detector (HPD), to detect photons created by particles traversing a radiative medium. The HPD uses the techniques of a photo-sensitive cathode and electron cross-focussing together with a hybrid pixel detector as the anode to create a low-noise device sensitive to single photons. This low noise allows the detector to be used efficiently in a pattern recognition system for identifying particles according to the angle of the Cherenkov photon ring they produce. This hybrid system also allows the detector to operate cleanly in the harsh environment of a hadron collider.

The full description of the pixel HPD can be found in Refs. [2,3]. Photons incident on an optical input window, ~8 cm in diameter, release a photo-electron from a photo-sensitive cathode layer deposited on the inner surface. These photo-electrons are accelerated to a high kinetic energy, typically 20 keV, and electro-statically focused onto an anode consisting of a silicon pixel sensor and readout chip assembly mounted on a ceramic pin-grid-array (PGA) carrier. An image at the photocathode is de-magnified by a linear factor of 5 by the electron optics. Connections between the silicon sensor and chip are made by micro-scopic solder bumps, one per pixel. Charge created by the photo-electron in the sensor is detected by the analog front end of the readout chip and converted to binary hit information. After subsequent processing, data are transferred from the device via the pins of the PGA carrier. In total, the LHCb RICH system will use 484 such HPDs, each providing 1024 channels of data.

The low noise of the device is due to the small capacitive load of the sensor pixel on its readout channel. Another advantage is the possibility of data processing on the chip which allows a fine segmentation of the active area into many small pixel channels whilst keeping the number of pins of the PGA to a level easily produced in industry.

*Tel.: +41 22 767 5903; fax: +41 22 767 8310.
E-mail address: ken.wyllie@cern.ch.

0168-9002/$ - see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2006.05.160

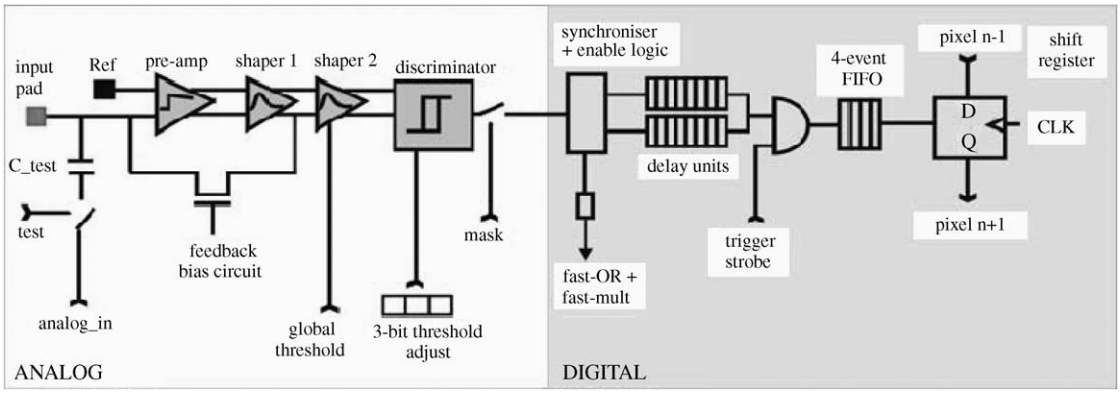

Fig. 1. Schematic of the pixel cell.

In the environment of LHCb, events will be accepted at a mean rate of 1 MHz. This means that a full event of HPD data must be read out within 1 μs. Data links are required that can transfer a total event bandwidth of 500 Gbit/s whilst tolerating the environment of LHCb.

2. LHCBPIX1 pixel readout chip

A complete list of the specifications of the pixel electronics is given in Ref. [1], but those most relevant to this paper are listed below. A photo-electron accelerated by a 20 kV potential should create a signal of ~5000 electrons in the pixel sensor. This is, however, reduced by effects such as back-scattering and charge-sharing between channels. The signal size to which the pixel should be sensitive, which is the minimum threshold for a binary system, is specified as 2000 electrons. The chip and the other components of the complete anode must function within the tube vacuum where the evacuation of heat is restricted and they must be compatible with all the manufacturing steps of the HPD. The electronics must also withstand some level of ionizing radiation, estimated at ~30 krad for 10 years of LHCb operation. It must also be insensitive to single-event-effects.

The front-end chip designed to meet these requirements is known as LHCBPIX1. It is fabricated in commercial 0.25 μm CMOS and takes advantage of the intrinsic radiation tolerance of modern sub-micron technologies whilst using special layout techniques to enhance its robustness [4]. In total, the chip contains 13 million transistors. When operated at full LHCb speed (40 MHz clock and 1 MHz trigger rate) it consumes 1.8 W of power. The overall digital architecture is the same as a previous version of the chip as described in Ref. [5].

The pixel matrix consists of 256 rows and 32 columns of 8192 pixels at a pitch of 62.5 and 500 μm, respectively. In the LHCb mode of operation, the data from eight adjacent pixels in a column are OR-ed together, effectively forming a super-pixel of dimension 500×500 μm. The matrix then consists of 32×32 super-pixels. This is described in detail in Ref. [5]. The circuit of one pixel is shown schematically in Fig. 1. The preamplifier and shaper circuits are differential to optimize the rejection of common-mode noise generated by digital switching. Shaper signals are compared with a threshold set globally across all the pixel cells and converted to a binary value by the discriminator. More details of the front end can be found in Ref. [6]. Hit information is buffered in the delay units until the arrival of the trigger, and then is written into a 4-event first-in-first-out (FIFO) memory. Data read from the FIFO are transferred into a single-bit register which, together with the other pixels in the column, form a shift register through which data are shifted out of the column. Data from the 32 columns are shifted out in parallel.

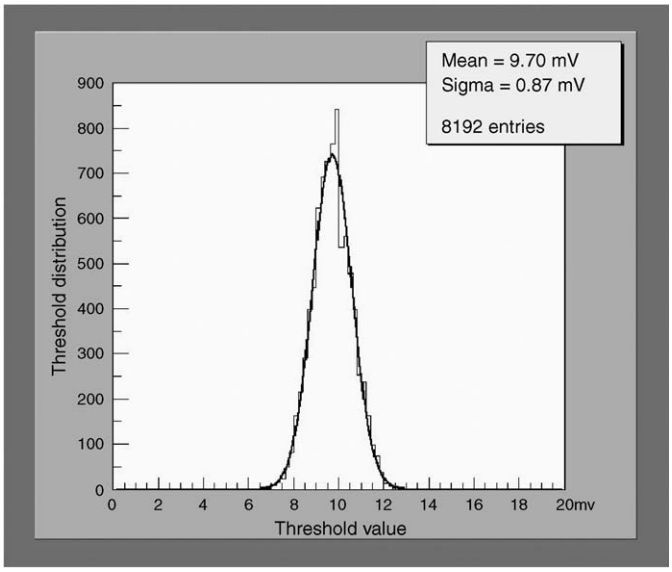

Fig. 2. Threshold distribution of the 8192 pixels of an LHCBPIX1 chip.

LHCBPIX1 has been tested extensively and meets all the requirements of LHCb. The performance of the front end and, in particular, the discrimination circuitry meets the specifications with a large margin. This is illustrated by Fig. 2 which shows the measured minimum thresholds across all 8192 pixels. Such a measurement is an indication of the sensitivity of the chip to photo-electron signals and