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A large dynamic range integrated front-end for photomultiplier tubes

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Abstract

A full custom analog CMOS circuit for obtaining a photomultiplier readout with a 16 bit resolution over 7 V has been developed. It is part of the R&D program for the photomultiplier tube front-end readout of the Pierre Auger Observatory northern site. It performs signal duplication and amplification with three gains: 0.15, 1 and 6. Each amplifier has a resolution of 10 bit and can measure signals with durations of several microseconds with a good baseline stability, for an input charge of up to tens of nano-Coulombs. The amplification is performed by current feedback amplifiers with a bandwidth of 60 MHz.The input impedance, adapted to the coaxial cables, is stable over the whole working range.

A prototype was submitted in April 2004 and successfully tested. The linearity over the working range is less than 1%. It was also successfully tested on the Auger surface detector element installed at Orsay (comprised of a Cherenkov water tank equipped with Photonis XP1805 9'' diameter photomultiplier tubes). The resolution over 7 V is 16.6 bit.This circuit is the first step towards a ''system-on-a-chip'' (SoC) solution for a photomultplier tube readout equipped with a fast ADC for signal digitization. A setup using a single cable for both the signal and the photomultiplier high voltage power supply was shown to be successful.

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Keywords: Front-end electronics; ASIC; Large dynamic range

1. Introduction

Astroparticle physics experiments require a large number of photomultiplier tubes (PMTs) for shape measurement over a large range in amplitude and time. This R&D program is being carried out with the needs of the northern site of the Pierre Auger Observatory [1] in mind. The aim is to produce a low-cost ''system-on-a-chip'' (SoC) solution for signal digitization over an equivalent number of 16 bit at a speed of 100 megasamples/s (MSPS). The results from the first phase of this program, the front-end electronics (FEE) developments, are presented in this paper. CMOS 0.35 μm technology was favored as it is regarded as a standard for analog circuits for the coming years.

The field of application is discussed from the northern Auger requirements and uses previous experience gained form the southern site production. The design and the results of tests on prototypes are then presented.

2. Field of application

The Pierre Auger Observatory uses 5000 photomultiplier tubes. They are grouped into clusters of three units. Each cluster manages the power supply and data transmission. The high-voltage (HV) supply and control, and the signal digitization is done on the same board and from the same low-voltage power supply (LV). This board is placed close to the photomultiplier tube. The digital signal transmission is then performed over long distances. For the northern site, the FEE, HV and LV functions are kept separate from the PMT, then, in case of a failure it is more efficient to replace only the electronics than the electronics with the tube. The above summarizes the basic criteria used in the R&D program.

The northern Pierre Auger Observatory will require an input dynamic range of 16 bit, and signal digitization over

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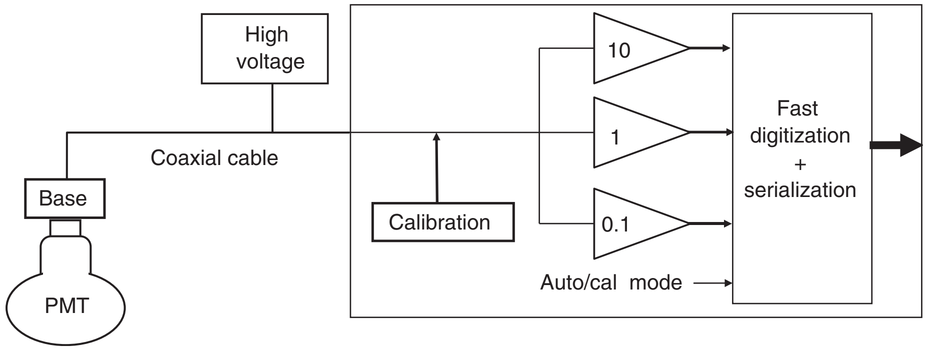

Fig. 1. Proposed architecture.

20 µs. The data analysis consists of studying pulses ranging from a few, to some millions of photoelectrons. The pulse frequency range was measured on a prototype of the Auger Surface Detector in Orsay [2] which detects cosmic rays by the Cherenkov effect in 12 m^3 of water. The Cherenkov light is collected with the PMTs. Since the photoelectron distribution can be studied from the pulses' trailing edges, their overall bandwidth was measured and found to range from 1 to 50 MHz.The minimum sampling frequency, calculated from Nyquist's theorem is 100 MSPS. Under nominal working conditions signal amplitudes can reach values of 150 mA (7.5 V on 50 Ohms) or more. This value was set as the upper working limit for the current development.

The solar cell power supplies require a stringent power management. Industrially manufactured HV power supply modules were successfully used in the southern Auger project [2]. For the northern site, a compromise between the ADC input power and consequent output per-formance is required. The solution presented here proposes to amplify the input on several ranges in order to work with 10 bit ADCs. The overlap necessary to ensure a good cross-calibration leads to the implementation of three different gain ranges (approximately 0.1, 1 and 10).

During the R&D and production phases of the PMT bases [2] the connectors were seen to be one of the most critical elements influencing the failure rate. The number of connectors will therefore be minimized by using the same coaxial cable for both the signal and the tube HV power supply.

The proposed architecture is summarized in Fig. 1. In order to reduce power dissipation, which arises mainly from the lines in the PCB (printed circuit board) driving the output buffers, the digitization and serialization will be implemented on the same chip. A reduced number of outputs also increases the reliability.

3. Design

A circuit with three amplifiers was designed. The principle is presented in Fig. 2. The main difficulty is to ensure a stable input impedance of the circuit and a linear behavior of nonsaturated channels whenever a given channel reaches its saturation level. Current feedback operational amplifiers (CFOAs) were chosen for this purpose as they maintain a high input impedance, even under saturation. The coaxial cable is terminated by an internal resistance. Its value (50 Ohm for the prototype presented) always remains much lower than the amplifier input impedance. This resistance also acts as a voltage divider and consequently, the design is reduced to only two types of CFOAs, namely a follower and a gain-10 amplifier. The bias voltage has to be regulated as it is sensitive to small voltage variations. This is achieved by using an operational transimpedance amplifier (OTA). The coupling capacitors are kept external in order to reach high values, and so baseline variations due to large signals are minimized. The capacitor coupled to ground must have a low current leakage and must also provide a low equivalent series resistance in order to prevent any modification in the CFOAs' bias voltage.

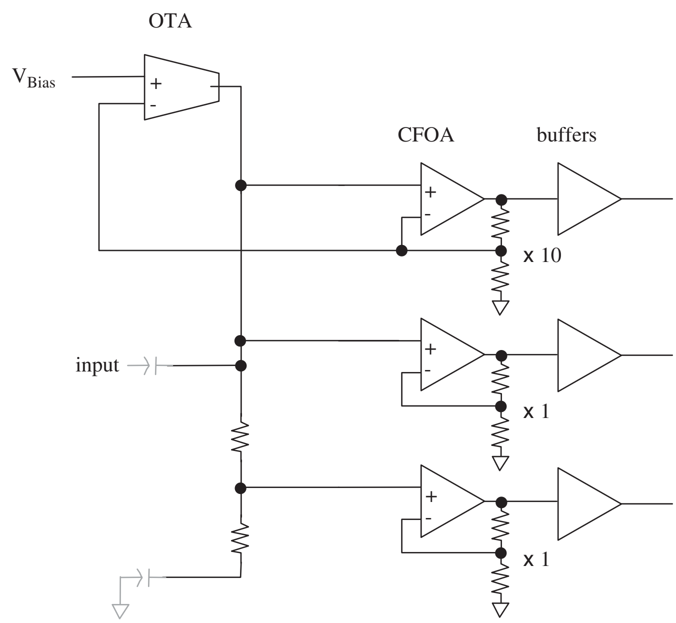

Fig. 2. Circuit principle.The external components (capacitors) are represented in gray.