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An improved PIN photodetector with integrated JFET on high-resistivity silicon

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Abstract

We report on a PIN photodetector integrated with a Junction Field Effect Transistor (JFET) on a high-resistivity silicon substrate. Owing to a modified fabrication technology, the electrical and noise characteristics of the JFET transistor have been enhanced with respect to the previous versions of the device, allowing the performance to be significantly improved. In this paper, the main design and technological aspects relevant to the proposed structure are addressed and experimental results from the electrical characterization are discussed.

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Keywords: Fabrication technology; Junction field effect transistors; Silicon radiation detectors; PIN photodetectors; Electrical characterization

1. Introduction

Silicon detectors are extensively used in many scientific, medical and industrial applications. They can be operated as stand-alone detectors for spectroscopy, or arranged in linear or 2D arrays for photon-imaging applications. Front-end transistors integrated on the detector chip may offer many advantages, owing to the optimized detector–preamplifier connection, and have been shown to be the best choice in terms of noise performance, especially in the case of detectors with low anode capacitance (a few hundreds of fF), such as silicon drift detectors and pixels [1,2].

In the past few years ITC-irst (Trento, Italy), in collaboration with some other research groups, has developed a technology for the fabrication of detectors and integrated electronics on high-resistivity silicon. In particular, we have already reported on a test structure consisting of a PIN diode coupled to a double-gate, n-channel Junction Field Effect transistor (JFET), allowing an innovative feedback scheme to be implemented in the charge preamplifier topology providing a continuous reset without feedback resistor [3]. Nevertheless, the performance of this device was degraded by the presence of excess white noise in the JFET, preventing the Equivalent Noise Charge (ENC) to reach its theoretical value (a minimum ENC of 60 rms electrons at room temperature was measured [4]).

The reason for this excess noise has been investigated both experimentally and with the aid of TCAD simulations, and could finally be ascribed to the depletion of the bottom-gate, whose doping profile was not adequately concentrated and deep. This caused a bias-dependent series resistance, that contributed thermal noise to the transistor. In order to fix the problem, a modified fabrication technology has been developed, allowing for a sizeable enhancement in the device performance.

In this paper, we report on the electrical characteristics of the PIN + JFET test-structure fabricated with this

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improved technology. The device is intended as a detector for X- and γ-rays as well as for visible light. In particular, we are investigating its operation as the core element of a γ camera for scintimammography, composed of a 2D array of detectors with 2 mm pitch, coupled to pixellated CsI(Tl) crystals able to convert ^{99}Tc 140 keV photons into light photons centered at 550 nm wavelength.

2. Device description

The test-structure consists of a PIN diode (0.8 mm^2) coupled to an integrated n-channel JFET in the double-gate (tetrode) configuration. The layout and the schematic cross-section are shown in Figs. 1 and 2, respectively: the diode p^+ region is connected to the JFET top-gate at the metal level. The JFET layout has a radial symmetry, the drain (*D*) being completely surrounded by the top-gate (TG), which in turn is surrounded by the source (*S*) and by the bottom-gate (BG) contact region. The latter can be biased independently from the top-gate, this allowing for double-gate operation. The top gate width and length are 100 and 6 μm, respectively. A 100-μm wide, p^+ implanted guard-ring (GR) surrounds the entire PIN + JFET structure, in order to properly shape the electric field and to collect the edge leakage current. The structure also includes an integrated feedback capacitor and a test (injection) capacitor (at the top-left and bottom-right corners of the diode in Fig. 1). A circular opening on the diode metal layer (300-μm diameter) allows for electro-optical testing.

An alternate layout version (layout 2) is also available, where a narrow floating p^+ guard-ring is present all around the PIN diode to reduce its parasitic capacitances toward the adjacent implants.

As reported in Ref. [5], the main characteristics of the fabrication process are: (i) p^+ and n^+ implants (shallow and deep) and thermal diffusion for the JFET realization and (ii) back-side, P-doped poly-Si gettering to ensure low diode leakage current.

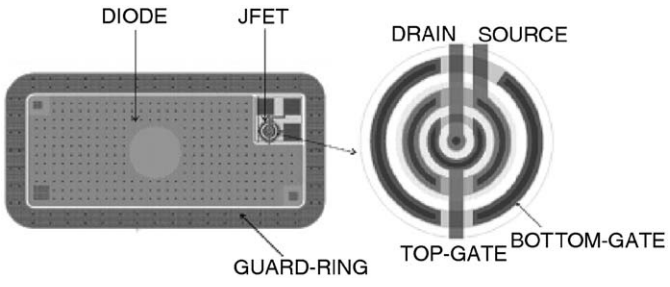

Fig. 1. Layout of the PIN + JFET structure, with JFET detail.

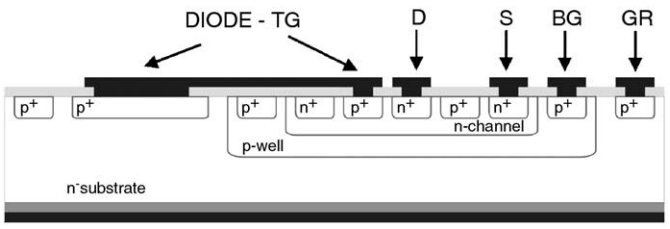

Fig. 2. Cross-section of the PIN + JFET structure (not to scale).

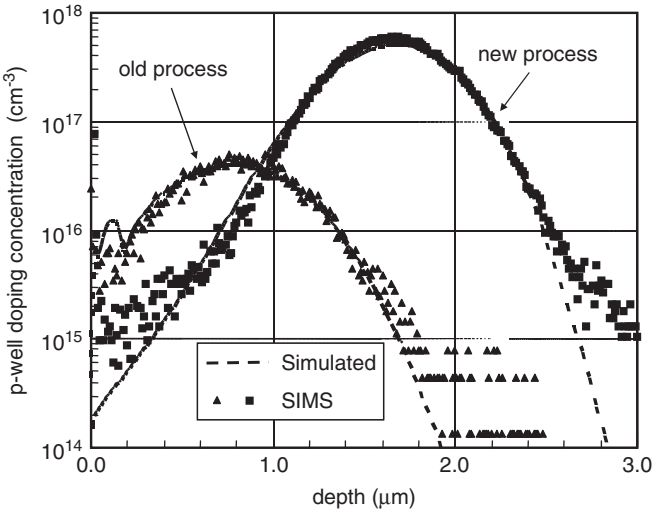

Fig. 3. P-well doping concentration profiles (measured by SIMS and simulated) for the old and new process.

Several non-idealities observed in the static and capacitance characteristics of the JFET transistors made from the old technology suggested that the p-well (bottom-gate) was depleted. To gain deep insight into this problem, we have carried out a thorough characterization work on the doping profiles, involving different measurement techniques [6], namely Secondary Ion Mass Spectroscopy (SIMS) and Spreading Resistance Measurements (SRP), in combination with process/device simulations [7]. The correct doping profiles could be reconstructed and later incorporated in device simulations, that were found to accurately reproduce the JFET characteristics and confirmed the malfunctioning of the p-well to be the origin of device non idealities [8].

Following the indications of the simulations, the fabrication technology has been modified: in particular, a high-energy (1 MeV) boron implantation with a higher dose has been implemented to obtain a much deeper, highly doped bottom gate. Fig. 3 shows the p-well boron concentration profiles extracted by SIMS for both the old and the new process, along with the simulated ones.

A new batch of devices has been processed with this modified technology on 100-mm diameter, FZ, 300-μm thick, $\langle 1\,1\,1 \rangle$ oriented, phosphorus-doped silicon wafers, with nominal resistivity of 6 kΩ cm.

3. Experimental results

Measurements on test structures confirmed the good process quality. Notably, the leakage current density is lower than 0.5 nA/cm^2 at full depletion. The depletion voltage was found to range between 35 and 70 V, depending on the considered wafer, so that an 80 V