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Functional testing of the ATLAS SCT barrels

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On behalf of the ATLAS SCT collaboration

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Abstract

The ATLAS SCT (semiconductor tracker) comprises 2112 barrel modules mounted on four concentric barrels of length 1.6 m and up to 1 m diameter, and 1976 endcap modules supported by a series of nine wheels at each end of the barrel region, giving a total silicon area of 60 m^2.

The assembly of modules onto each of the four barrel structures has recently been completed. In addition to functional tests made during the assembly process, each completed barrel was operated in its entirety. In the case of the largest barrel, with an active silicon area of approximately 10 m^2, this corresponds to more than one million instrumented channels.

This paper documents the electrical performance of the four individual SCT barrels. An overview of the readout chain is also given.

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1. Introduction

ATLAS [1] will be the largest detector to operate at CERN's Large Hadron Collider (LHC). The ATLAS SemiConductor Tracker (SCT) is part of the ATLAS Inner Detector. The SCT Barrel comprises four concentric barrels of length 1.6 m which support a total of 2112 barrel modules. The two SCT Endcaps each comprise a series of nine disks supporting a total of 988 endcap modules. This paper documents the "as built" performance of the four SCT barrels and the techniques used to test the modules.

1.1. The barrel module

The ATLAS SCT Barrel Module [2] comprises a VHCPG (Very High Thermal Conductivity Pyrolitic Graphite) baseboard glued between two planes of single sided silicon microstrip detectors. Each plane comprises a pair of AC coupled p-in-n silicon sensors with 80 μm strip pitch, produced by Hamamatsu Photonics [3]. Small angle stereo geometry is used to provide positional information in two dimensions, an angle of 40 mrad being engineered between the two sides.

Each module is read out by 12 ABCD3TA ASICs [4] mounted on a copper/kapton hybrid [5]. Manufactured in the radiation hard BiCMOS DMILL process, each chip provides sparsified binary readout of 128 channels. The amplified and shaped input signal is compared to a programmable threshold having two components: a single 8-bit DAC applied across the whole chip, and a channel specific 4-bit (trim) DAC designed to compensate for channel-to-channel variations. The resulting hit pattern is transferred into a binary pipeline, 132 cells deep. Upon receipt of a Level 1 Accept (L1A) trigger, the pipeline output is transferred into a derandomising buffer that can store up to eight events. In addition the ASIC has a four bit L1A counter and an eight bit Bunch Crossing (BC) counter: the output data includes a record of these counters such that data from all parts of the SCT may be assembled into one event record. The design also includes charge injection circuitry to facilitiate calibration of the front end.

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1.2. Barrel services

Electrical and optical services are brought to the modules by means of "harnesses". Each harness comprises six doglegs, six pairs of Low Mass power Tapes (LMTs), 12 data fibres and six control fibres.

The clock and command signals are transmitted to the module in the form of a biphase mark encoded optical signal [6]. This is received by a PIN [7] diode and converted into separate LVDS[1] clock and command signals by the DORIC [8] chip. In turn the module generates two LVDS data streams, each one being used by the VDC [8] chip to modulate the output of a VCSEL [9] diode such that data are sent off-detector in optical form. Hence each module is associated with three optical fibres which terminate in an opto package mounted on the dogleg. This package houses the DORIC and VDC chips in addition to the PIN and VCSEL diodes.

An evaporative cooling system is used to remove the heat generated by operation of the SCT. One barrel cooling unit services 48 modules (four rows). The two inner rows of each cooling unit end in a common outlet manifold, the two outer rows being inlets, connected directly to capillliaries. At the end of each outlet row, just before the manifold, a pair of thermistors is attached to the pipe. In addition to the provision of temperature monitoring, these also serve as inputs to the power supply interlock system such that, if the cooling system may fail, the power is cut off to prevent overheating of the detector modules [10].

1.3. Macro-assembly

Barrel modules were shipped to the macro-assembly site from each of the four production clusters and were tested upon receipt to verify that they had not been damaged in transit. Based upon these electrical results, and results from the production cluster, modules were carefully graded and selected to be mounted on each barrel.

A pair of custom robots [12] were used to locate the detector modules onto the barrels. This choice was made primarily due to the very restricted clearances between each module, its neighbours and their support structures, which dictated that each module could only be moved into position by following a tightly controlled path [11]. Before each module is mounted, a carefully controlled layer of thermal grease is spread onto the cooling block, part of the cooling unit, to ensure good thermal contact is made. Fig. 1 shows the last module being mounted onto barrel 3, the innermost barrel and the first to be completed.

At the peak of the macro-assembly programme, running two shifts, each robot could mount 36 modules per day. Only five modules were damaged during macro-assembly (0.2%). In the event that after electrical testing a module needed to be removed and replaced, this was also done by means of the robot.

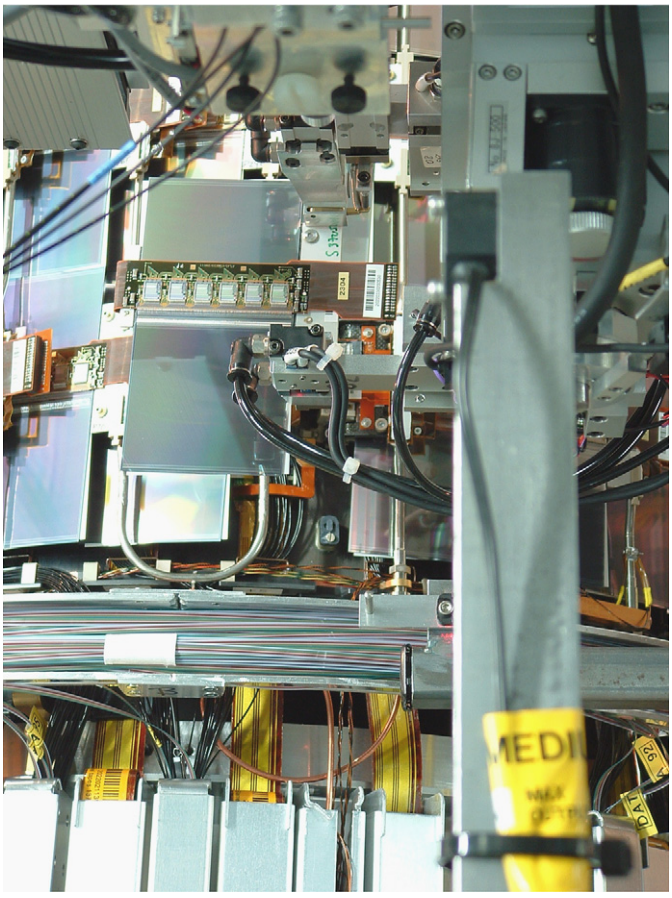

Fig. 1. Mounting the last module on Barrel 3.

1.4. Data acquisition system

The module power supplies [13] and readout hardware used were a subset of those to be used in ATLAS. Macro-assembly provided the first opportunity to use these systems on a large scale.

The Data Aquisition System (DAQ) is centred around the ATLAS Silcion/Pixel Read Out Driver, (ROD) a 9U VME64X module common to both subdetectors. This comprises five Digital Signal Processors and memory in addition to several functional blocks implemented within Field Programmable Gate Array logic. Each ROD is connected to a Back Of Crate card (BOC) which provides the interface between the electrical and optical domains: different versions of the BOC exist for the SCT and Pixel subdetectors. Within each readout crate there is also a Timing Interface Module (TIM), which distributes clock and trigger information to the RODs by means of a custom crate backplane, and a Single Board Computer which communicates with TIM and the RODs by means of the VME bus.

Each ROD has four Slave DSPs and one Master DSP. The MDSP is used to broadcast L1A triggers to the

[1]Low voltage differential swing.