Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 570 (2007) 317–321
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

First electrical characterization of 3D detectors with electrodes of the same doping type

Alberto Pozza[a,*], Maurizio Boscardin[a], Luciano Bosisio[b], Gian-Franco Dalla Betta[c], Claudio Piemonte[a], Sabina Ronchin[a], Nicola Zorzi[a]

[a]*Divisione Microsistemi, ITC-irst, Via Sommarive 18, I-38050 Povo, Trento, Italy*
[b]*INFN and Dipartimento di Fisica, Università di Trieste, Via A. Valerio, 2, I-34127 Trieste, Italy*
[c]*INFN and Dipartimento di Informatica e Telecomunicazioni, Università di Trento, Via Sommarive 14, I-38050 Povo, Trento, Italy*

Available online 2 October 2006

Abstract

The 3D silicon radiation detectors are very promising devices to be used in environments requiring extreme radiation hardness, such as the super-LHC experiment at CERN. A drawback of this detector is the very long and non-standard fabrication process, which makes the mass production of these devices very critical. A possible simplification of the manufacturing process relies on a new type of 3D architecture, called 3D-single-type-column detector, that we have introduced in previous works. In this paper we report on the fabrication process of the first batch of detectors and on selected results from the electrical characterization of 3D test structures, covering leakage current, capacitance and breakdown voltage measurements.

PACS: 29.40.Wk; 29.40.Gx; 85.30.De

Keywords: Silicon detectors; Fabrication technology; Electrical characterization; 3D detectors; DRIE etching

1. Introduction

In the mid-nineties a new architecture of silicon radiation detectors, called 3D detector, was proposed [1], which involves the fabrication of the electrodes deep inside the silicon wafer. This detector concept has soon given rise to a great interest because of its intrinsic advantages over standard planar detectors. Indeed, due to the fact that the electrode distance depends on the layout, rather than on the wafer thickness, it is possible to shorten the electrode distance allowing for low depletion voltage and fast charge collection times. It is important to note that, differently from thin detectors, this is obtained without reducing the amount of signal charge released by a particle, that scales with the substrate thickness. In heavily irradiated planar detectors the increase of the depletion voltage and the reduction of the charge carrier mean drift length due to trapping effects are a major issue [2]. In 3D detectors, a direct consequence of the low depletion voltage and short distance between electrodes is an increase of the radiation tolerance.

A drawback of 3D detectors is the rather long and complex fabrication process, as methods of silicon micromachining must be used. This could lead to the unfeasibility of mass production of these detectors. In our previous works [3,4] we described a new architecture of 3D detector, called 3D-single-type column (3D-stc), whose main purpose is the simplification of the fabrication process. This device consists of columnar electrodes of one doping type only, e.g., n^+ columns on a p-type substrate, which is the case of our first production batch. Owing to the single column etching and doping step, the fabrication process of these devices is much simpler. Moreover, if columns are only partially etched through the wafer thickness, an additional simplification is related to the fact that no support wafer during processing is necessary and the ohmic electrode can be obtained by

*Corresponding author. Tel.: +39 0461 314438; fax: +39 0461 302040.
E-mail address: albpozza@itc.it (A. Pozza).

0168-9002/$ - see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2006.09.032

means of a uniform implant/diffusion on the back side of the wafer.

For the sake of completeness, it is worth citing that similar devices (namely 3D detectors featuring p^+-doped columns on n-substrates) have been independently developed by another group in Finland [5]. With respect to such devices, in our detectors, featuring n^+-doped columns on p-substrate, an additional process step is necessary to interrupt the inversion electron layer, formed by the positive fixed oxide charge, between the n^+ electrodes at the surface. Despite this complication, a definite advantage is expected in case of high irradiation levels causing severe charge trapping problems since the collected carriers are the electrons, which feature a higher electron mobility with respect to holes.

A side disadvantage of 3D-stc detectors with respect to the original double-type-column design is the impossibility to control the electric field strength acting on the applied voltage. In fact, once full depletion is reached, the electric field in the inter-column region cannot be increased by increasing the reverse voltage further, and the peak electric field depends on the value of the substrate doping concentration only. As a consequence, the electric field in the middle of the region between two columns can be low, as also evidenced by TCAD simulations [3].

In this paper we report experimental results from the electrical characterization of the first batch of 3D-stc detectors manufactured at ITC-irst, Trento, Italy, along with a description of the device layout and of the fabrication process. Measurement data from a specially designed 3D test structure, including leakage current, breakdown voltage and capacitance are presented and discussed.

2. Fabrication technology and device layout

2.1. Fabrication

The first batch of 3D-stc detectors has been fabricated on p-type, $\langle 100 \rangle$-oriented, high-resistivity substrates belonging to two different ingots:

- Float Zone (FZ) wafers, with a nominal resistivity of 5 kΩ cm and a 500 μm thickness.
- Czochralsky (CZ) wafer, with a nominal resistivity > 1.8 kΩ cm and a 300 μm thickness.

With reference to Fig. 1, showing a Scanning Electron Microscope (SEM) micrograph of a device cross-section, the fabrication technology can be outlined as follows. First of all a screen oxide is grown and boron implantation is performed both on the back side, to obtain the p^+ ohmic contact, and on the front side to provide electrical isolation between columns. Either p-stops (patterned implant) or p-spray (blank implant) have been used in the first batch for this purpose. Then, a carefully dimensioned passivation is realized on the front side, and holes are etched by means

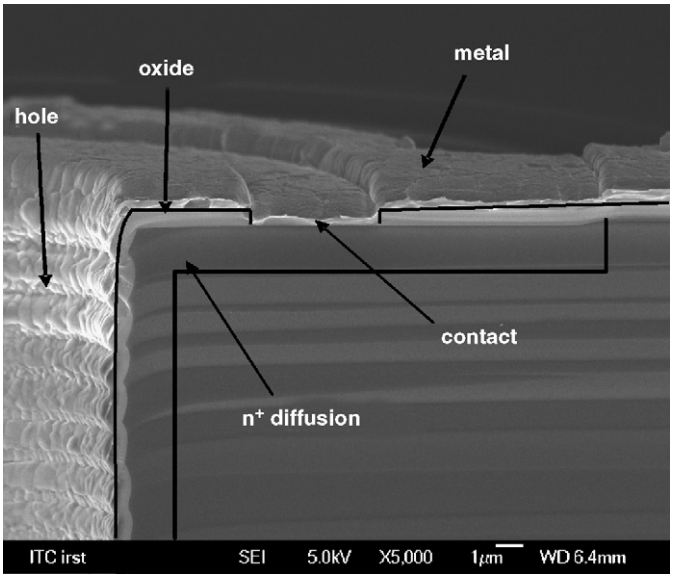

Fig. 1. SEM micrograph showing a detail of a 3D-stc device.

of Deep Reactive Ion Etching (DRIE) technique (this step has been performed at CNM, Barcelona, Spain). Holes having a diameter in the range from 6 to 10 μm and a maximum depth of 150 μm were etched in the first batch. Subsequently, holes are doped using a solid source of phosphorus to form the n^+ electrodes, and then they are passivated and partially filled by growing an oxide layer. Finally, contacts are defined and etched in the region around the top of the holes (also doped with phosphorus) and aluminum is sputtered.

2.2. Layout

The wafer layout used for the first batch of 3D-stc devices includes test structures, both standard planar and 3D devices, and 3D detectors in a strip-like configuration.

The standard planar structures consist of diodes with guard rings, gated diodes and MOS capacitors and are used to control the quality of the process, while the 3D test devices consist of both one-column structures and matrices of columns. In order to ease the electrical tests and the bonding to standard read-out chips for functional characterization, column matrices are arranged in a strip detector fashion, i.e., with all columns belonging to one row connected together (at the metal and/or at the n^+ surface diffusion level), with pads at the end of the rows for probing and bonding purpose.

Moreover, a special 3D test structure has also been designed, that we called 3D diode. As an example, Fig. 2 shows the layout of one of these devices. It consists of an inner matrix of 10×10 columns that can be biased together as one electrode owing to a metal line connecting all the outer columns and to the n^+ diffusion strips connecting rows of inner columns. This 10×10 column matrix is the 3D diode; around it are a first p-stop, whose purpose is to isolate the n^+ column matrix from its guard ring, and two