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CCD developments for particle colliders

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Abstract

Charge Coupled Devices (CCDs) have been successfully used in several high-energy physics experiments over the last 20 years. Their small pixel size and excellent precision provide superb tool for studying of short-lived particles and understanding the nature at fundamental level. Over the last years the Linear Collider Flavour Identification (LCFI) collaboration has developed Column-Parallel CCDs (CPCCD) and CMOS readout chips to be used for the vertex detector at the International Linear Collider (ILC). The CPCCDs are very fast devices capable of satisfying the challenging requirements imposed by the beam structure of the superconducting accelerator. First set of prototype devices have been designed, manufactured and successfully tested, with second-generation chips on the way. Another idea for CCD-based device, the In-situ Storage Image Sensor (ISIS) is also under development and the first prototype is in production.

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1. Introduction

The International Linear Collider (ILC) is widely accepted as the next big particle accelerator after the Large Hadron Collider (LHC), currently being built at CERN. As a machine designed for precision physics measurements the ILC will require a vertex detector with excellent performance to achieve its full potential. Accurate reconstruction of decay chains, pure and efficient b and c tagging and vertex charge measurements will help unravel complex new phenomena like the anticipated Supersymmetry.

The vertex detector at ILC will have to be significantly better than the most accurate of its kind ever built, the VXD3 vertex detector [1]. Charge Coupled Devices (CCDs) were used as detector elements in VXD3, and CCDs have proven their potential in several successful applications in both collider and fixed target high energy physics experiments over the last 20 years.

CCDs are well suited for linear collider environments because of the much cleaner interactions and low backgrounds compared to those at hadron colliders. The very small CCD pixels allow excellent spatial resolution and two-track separation. This is helped by the low power dissipation, allowing the use of extremely low mass support mechanics. Large granularity, e.g. 2500 pixel/mm^2, permits integration of many events without loss of information due to overlaps. A diagram of the proposed CCD-based vertex detector for the ILC is shown on Fig. 1.

2. CCDs as particle detectors

2.1. Brief history

The use of the CCDs in particle physics started in the early 1980s, shortly after the first devices achieved maturity for commercial production. The chips were fairly small, about 1 cm^2, but even then the pixel size of $20 \times 20\,\mu\text{m}^2$ was far superior to any other semiconductor detector. The first application was in the NA32 fixed target experiment at CERN in 1984, followed by the VXD2 vertex detector, built for the Stanford Linear Collider with the same CCDs in 1992. The next generation upgrade detector VXD3 was

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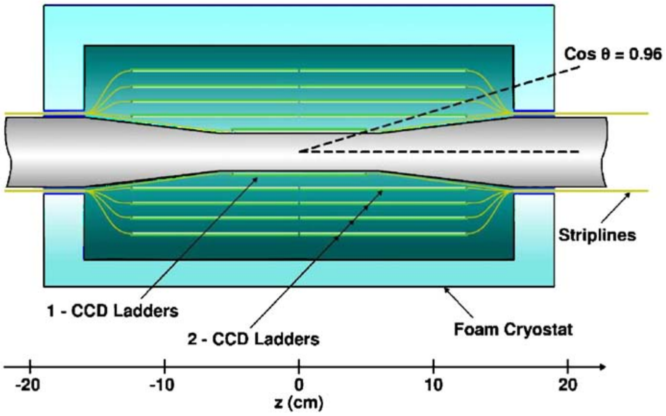

Fig. 1. Cross-section view of the proposed CCD-based vertex detector for the ILC.

built in 1996 with large custom CCDs of size $80 \times 16\,\mathrm{mm}^2$, arranged in 3 layers and had 307 Mpixel in total. Material budget of only 0.4% radiation length (X_0) per layer was achieved due to the use of thinned devices and beryllium support. Due to its small pixels and reduced multiple scattering the VXD3 was able to achieve excellent impact parameter resolution, still unsurpassed today.

2.2. *Performance*

CCDs have numerous advantages as particle detectors. Pixel size could be very small but usually $20 \times 20\,\mu\mathrm{m}^2$ is sufficient to achieve the resolution needed for a vertex detector. Modern semiconductor technology has produced CCDs with pixels as small as $1.56 \times 1.56\,\mu\mathrm{m}^2$ [2].

The sensitive epitaxial layer is usually quite thin, of the order of 20 μm. Extremely low mass detectors are possible if the sensor is thinned down to the edge of the epitaxial layer. Minimum Ionizing Particles (MIP) deposit on average 80 electron–hole pairs per micrometer of track which results in relatively small signal, however, excellent signal-to-noise ratio can be achieved due to the low readout noise. Charge is transported from one pixel to the next without introducing noise, which arises only at the output stage during conversion to voltage and buffering by a source follower. Readout noise of below 10 electrons ENC is routinely achieved at clock speeds of 1 MHz.

Very good spatial resolution can be achieved with CCDs because sizeable fraction of the charge is allowed to spread by diffusion in the non-depleted part of the epitaxial layer. The resulting charge sharing allows the use of the centre of gravity method for better positional measurement. For example, point resolution of 3.5 μm has been achieved at NA32 [3].

Full-Frame CCDs offer 100% fill factor and excellent uniformity in response and gain, which is essential for particle physics applications. In addition modern CCD technology allows the manufacture of large wafer-scale devices, which simplifies the mechanical design of detectors and is important for experiments requiring large sensitive areas.

2.3. *Limitations*

Charge transport is one of the most attractive features of the CCD because it allows the signal to reach one single output. This is at the same time a major weakness in radiation environments. Charge could travel several centimeters from the place it originated to the output and there is high probability of encountering bulk defects, generated by radiation damage. The effects of charge trapping could be reduced by device design and by carefully choosing the operating temperature and timing [4], but could pose limits particularly for large CCDs.

Despite the numerous advantages, CCDs do have their limitations [5]. The source followers need supply in the range 15–20 V and the power dissipation in the CCD outputs could become significant if many transistors are used. However, little power is dissipated in the image area of the device, which allows low mass gaseous cooling. In addition CCDs need numerous bias voltages, which complicate their use. The integration of on-chip CMOS electronics is difficult due to incompatibilities between the two processes. Another problem for high-speed applications is the large capacitance of the CCD image area, which is a challenge to drive because of the large currents involved.

2.4. *Principles of operation*

The CCD is an array of MOS capacitors, under which potential wells allow charge, which could even be a single electron, to be collected and stored. Due to the coupling between adjacent capacitors charge can be transported from one gate to the next with negligible losses, and upon reaching the output can be converted to voltage on a floating reverse-biased pn junction. The output node is reset by a transistor switch to a stable reference voltage and then disconnected before the charge reaches it. The arriving electrons decrease the potential on this floating diode, and the voltage step represents the output signal. An excellent overview on the principles and performance of modern CCDs can be found in Ref. [6].

Practically all CCDs used today are of buried channel type (BC CCD) to avoid charge trapping at the interface between the epitaxial silicon and the gate dielectric. The most common BC CCD is built on a high quality p-type epitaxial layer, onto which a profiled n-type dopant is implanted to form the buried channel. Upon depletion, the potential maximum under a gate occurs at a fraction of a micron below Si–SiO_2 interface, away from the defects present there. Small charges like those typical in particle physics applications would have been completely lost if the charge were allowed to come in contact with the Si–SiO_2 interface. Fig. 2 shows the potential profile in depth of a typical BC CCD.

The electrons are collected in the potential wells under the gates by drift while the holes are dumped to the substrate. If the epitaxial layer is not fully depleted the