Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 565 (2006) 165–171
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

The MOS-type DEPFET pixel sensor for the ILC environment

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Available online 12 June 2006

Abstract

A new generation of MOS-type DEPFET active pixel sensors in double metal/double poly technology with ~25 μm pixel size has been developed to meet the requirements of the vertex detector at the International Linear Collider (ILC). The paper presents the design and technology of the new linear MOS-type DEPFET sensors including a module concept and results of a feasibility study on how to build ultra-thin fully depleted sensors. One of the major challenges at the ILC is the dominant e^+e^- pair background from beam–beam interactions. The resulting high occupancy in the first layer of the vertex detector can be reduced by an extremely fast read out of the pixel arrays but the pair-produced electrons will also damage the sensor by ionization. Like all MOS devices, the DEPFET is inherently susceptible to ionizing radiation. The predominant effect of this kind of irradiation is the shift of the threshold voltage to more negative values due to the build up of positive oxide charges. The paper presents the first results of the irradiation of such devices with hard X-rays and gamma rays from a ^{60}Co source up to 1 Mrad(Si) under various biasing conditions.

PACS: 29.40.Gx; 61.82.Fk; 85.30.De

Keywords: DEPFET; APS; ILC; Vertex detector; Radiation tolerance; Ionizing radiation

1. Introduction

Higgs, SUSY and heavy-flavor physics are central themes in future linear colliders. They require precise vertexing and b-quark tagging using low-momentum tracks. As a consequence the tracking detectors have to be put as close as possible to the primary interaction point and the multiple scattering has to be kept as small as possible. Fine granularity pixel detectors and sufficiently high readout speed are required in order to resolve closely spaced tracks and in order to limit occupancy to a tolerable level. Power consumption has to be kept small in order to avoid the introduction of additional material for cooling. In the following, a solution that is able to meet these requirements is presented. It is based on the DEPFET structure [1], a concept which fulfills the function of detector and amplifier simultaneously. The DEPFET can be used as the first amplification stage in the center of a Silicon Drift Detector [2] or as a pixel cell in matrices designed for a variety of applications ranging from X-ray spectroscopy and imaging [3] to tracking of charged particles for the future International Linear Collider (ILC). This paper presents in Section 2 briefly the main features of the MOS-type DEPFETs designed for the ILC vertex detector, together with our approach for the

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doi:10.1016/j.nima.2006.05.045

production of thin wafer-scale matrices. Section 3 addresses the tolerance of MOS-type DEPFETs against ionizing radiation.

2. The DEPFET pixel cell and module concept

The vertex detector for the ILC (see e.g. Ref. [4] for further details) will be a set of cylindrical detectors arranged in ladders around the interaction point.

Each ladder is an array of pixel cells read out at the end of the ladder outside the sensitive volume. In the case of a DEPFET as the pixel cell, the signal charge is measured in every pixel on a row-by-row basis and the DEPFETs are successively switched on by means of gating lines controlled by shift registers located at the long side of the ladder.

The MOS-type DEPFET is integrated on a fully depleted silicon substrate. All the charge generated by a traversing particle drifts due to the electric field configuration inside the device toward the surface and is collected in a potential minimum for electrons underneath the external gate of the DEPFET. The charge cloud is stored and modulates the current in the channel of the FET which forms in this way the first amplification stage. After signal read out is finished, the charge is removed by applying a positive voltage to the 'Clear' contact (see Fig. 1). The combination of the detector material and first amplification stage in one single device has a number of advantages. The sensitivity of the entire bulk and the low capacitance of the read out node enable low-noise operation over a large range of temperatures. This is of particular interest for applications at linear collider experiments where the sensors have to be as thin as possible. A second important point is that the charge is measured at the place of generation and need not be transferred to the readout nodes at the edges of the sensitive region (like in CCDs), so trapping due to bulk damage by non-ionizing energy loss (NIEL) is of minor importance. And finally, since the transistors can be turned off during charge collection and since only one row is electrically active during read out, the expected power consumption in the sensitive area is extremely low. Assuming $I_D = 30\,\mu A$ at $V_{DS} = -5\,V$ for the DEPFET pixel during read out, we expect a total power dissipation of about 21W for the 120 modules with roughly 800 Mpix in the sensitive DEPFET pixel area of the entire vertex detector. This is reduced by a factor 1/200[4], taking advantage of the duty cycle at the ILC. In addition to this, there is the power dissipated by the external steering and read out chips [5].

In our concept the DEPFET pixel array is made on thin (50 μm) detector-grade silicon supported by a directly bonded silicon frame of 300 μm thickness. Fig. 2 shows the sketch of such a module for the innermost layer at the ILC. The averaged material contribution of the ladder in the sensitive area is 0.11% X_0, including the frame and the (also back thinned to 50 μm) steering chips at the edge. The details of the read out and steering chips as well as the system aspects can be found in Refs. [5,6]. The latest results of system and beam tests will be the topic of a dedicated paper at this conference [7].

2.1. DEPFET technology and single pixel results

Fabrication of large wafer-scale pixel matrices demands a fault tolerant and reliable technology. The availability of more than one metal layer is mandatory due to the necessity of the row- and column-wise connections of the pixels. As a result, a new technology with two poly-silicon and two metal layers was introduced at the MPI Semiconductor Laboratory [8]. In order to guarantee a high homogeneity with respect to the operating parameters of the individual cells of the entire matrix, a MOS-type DEPFET was chosen as the pixel cell. Fig. 3 shows a cross-section through a DEPFET cell perpendicular to the transistor channel leading from the p-doped channel (right) to the n^+-doped clear contact. The n-doped internal gate is

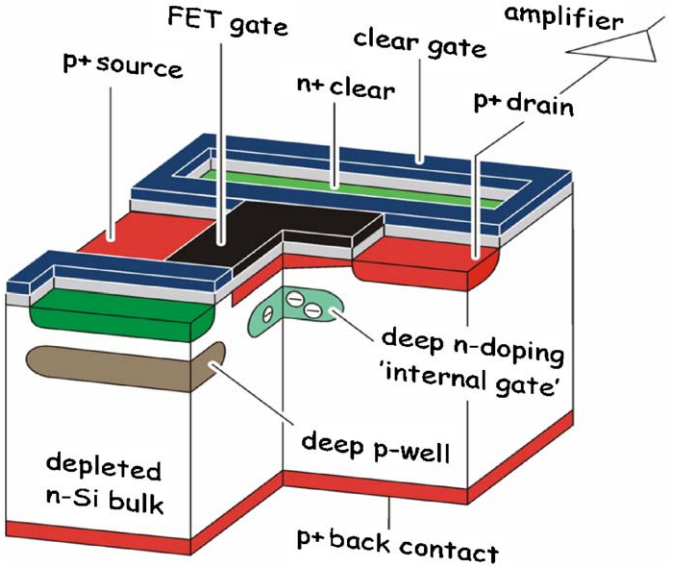

Fig. 1. Linear DEPFET topology for linear collider application.

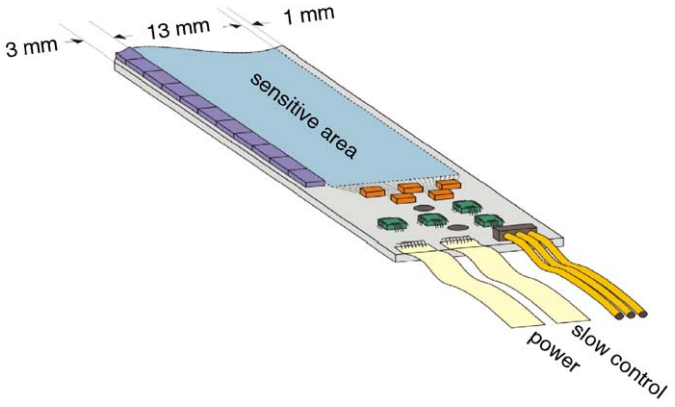

Fig. 2. Module concept for the first layer of the vertex detector at the ILC.