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First test beam results on DEPFET pixels for the ILC ☆

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Abstract

By incorporating a field effect transistor into a fully depleted sensor substrate the DEPFET sensor combines radiation detection and amplification in each pixel, resulting in very low noise and high spatial resolution. This makes DEPFET sensors a favorable technology for the vertex detector at the planned International Linear Collider (ILC). A prototype system with fast steering chips, a current-based readout chip and a 64×128 pixels DEPFET matrix has been built and was operated successfully in the DESY test beam. First results of the studies on two different DEPFET design options are presented in this paper.

Keywords: DEPFET; International linear collider (ILC); Vertex detector; Active pixel sensor; Beam test; Tracking

1. Introduction

The proposed International Linear Collider (ILC) offers vast prospects of precision measurements complementary to the discovery potential of the Large Hadron Collider (LHC). To fully exploit the physics potential a vertex detector with unprecedented performance providing pure and efficient b and c tagging is essential. Therefore, small pixel sizes of about $25 \times 25\,\mu m^2$ are necessary to achieve an excellent spatial resolution of a few micron. Furthermore, it is necessary to position the innermost layer as close as possible to the interaction point. Here, due to the dominating e^+e^- bremsstrahlung background ($80\,hits/mm^2/bunch\,train$) multiple readouts per bunch train (10–30 times) are required to keep the occupancy at a reasonable level. Therefore, line rates of several tens of MHz are necessary to read out the entire vertex detector, which contains almost 10^9 pixels, in $40\,\mu s$. Furthermore, the pair production background requires the detector to be radiation hard up to 250 krad. To keep the amount of material inside the vertex below 0.1% X_0 per layer, thin sensors with extremely low power dissipation to avoid active cooling are needed [1].

The DEPFET technology is a promising candidate for the vertex detector at the ILC.

2. Concept of a DEPFET microvertex detector for ILC

2.1. The DEPFET principle

By integrating a field effect transistor inside a fully depleted high resistivity sensor substrate a first amplification stage inside the pixel is realized [2]. Sideward depletion and an additional n-implantation below the FET create a potential minimum underneath the transistor channel working as a second, internal gate. Electrons created by an impinging particle are accumulated in the internal gate, thus changing the potential of the internal gate and thereby modulating the transistor channel current. As the charge collection still continues while the transistors are switched off, dead time and power consumption can be held extremely low. Due to the non-destructive readout the

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charge in the internal gate has to be removed by an external reset mechanism, also called the clear of the internal gate. This is done by applying a positive voltage pulse at the clear contact, which is included in each pixel. A MOS structure (Clear-Gate), which facilitates the clear process, is either clocked row-wise or held at a constant potential throughout the matrix. The reliability of the clear mechanism has already been proven [3].

The DEPFET pixel matrix is operated in a row-wise readout scheme: a row is selected by applying the voltage to the external gate of the pixels cells in that row. After probing the current of that row, the charge in the selected row is removed by applying the clear mechanism. Next the pedestal currents are sampled.

It has been shown that DEPFET pixels are radiation hard up to 1 Mrad (SiO_2) [5] and that thinning of DEPFET pixels down to 50 μm is feasible [4]. The expected power consumption of a five layer DEPFET vertex detector is less than 5 W [6] and therefore active cooling is very likely not required, leading to a material budget of about 0.1% X_0 per layer.

One promising design option is a sensor with an additional unmasked, deep, high energy phosphorous doping (see Fig. 1). In those so-called 'high E' structures the clear process, which is mainly a punch through from the clear region towards the internal gate, takes place about 1 μm depth below the interface. This leads to a significant reduction of the required clear potential. On the other hand, the internal gate is also located deeper in the bulk. This results in a lower capacitive coupling to the transistor channel and thus a lower internal gain of around −20%.

Measurements show that complete clearing can be obtained over a large parameter range and that the required voltage swing is as low as 5–7 V for the matrix with high E implantation compared to 12–14 V for the standard sensor [3]. Furthermore, an operation with a constant clear-gate potential is possible. These features have impact on various aspects. Firstly, the number of switching channels is reduced and thus simplifies the sensor and system design considerably. Secondly, as the radiation tolerance of the SWITCHER chip with its presently thick gate oxides (required for 'high voltage' operation) may be insufficient, these low clear voltage steps will allow the use of standard CMOS technologies with better radiation tolerance.

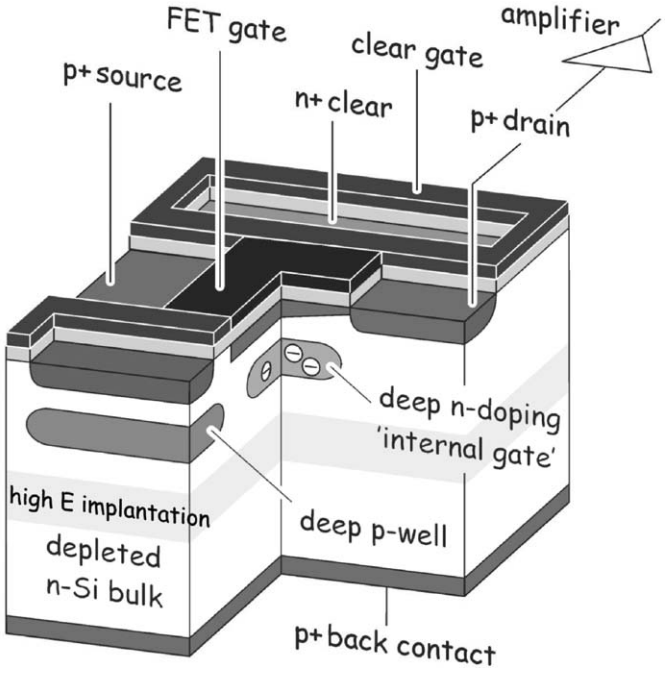

Fig. 1. Schematic cross-section of a DEPFET pixel cell with additional high energy implantation.

2.2. The DEPFET ILC prototype system

The ILC DEPFET-System [7] consists of two major parts, a sensor PCB and a stack of DAQ-boards. The DAQ-boards are responsible for configuring the steering and readout chips and for digitizing and storing the analog data. Furthermore, it provides an USB based communication with a DAQ-PC. The sensor PCB hosts the 64 × 128 DEPFET pixel matrix, the two steering chips SWITCHER II and the readout chip CURO II. The SWITCHER II chips are placed on each side and have the purpose of steering the DEPFET matrix in terms of row selection and clearing. The CURO II (CUrrent Read Out) samples the current of the matrix columns in parallel and has on-chip pedestal subtraction, zero-suppression and hit-finding.

3. Test beam setup

The test beam measurements have been carried out with a 6 GeV/c electron beam.

The Bonn ATLAS telescope (BAT) was used to reconstruct the tracks [8]. It consists of four identical planes of double-sided silicon microstrip detectors with a pitch of 50 μm (without intermediate strips). The trigger signal is provided by a coincidence of two scintillators.

The CUROs ability of zero suppression was not used, thus reducing the readout speed to a line rate of 36 kHz.

Two DEPFET matrices with 64 × 128 rectangular pixels with a pixel size of 36.0 × 28.5 μm^2 have been studied. The sensor thickness is $d = 450$ μm. One of the two sensors has a high energy implantation.

The sensors were operated fully depleted, with backplane voltages of $V_{bp} = -120$ V for the sensor with high-E and $V_{bp} = -160$ V for the one without high-E, respectively.

The analysis of the data presented in this paper is based on a fiducial of 30 × 30 pixels which did not contain pathologically noisy pixels.

4. Measurements with non-high-E sensor

4.1. Data processing

The off-line processing of the raw data is done by subtracting the pedestals, which are calculated as the