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Flip chip bumping technology—Status and update

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Abstract

Flip chip technology is a key driver for new complex system architectures and high-density packaging, e.g. sensor or pixel devices. Bumped wafers/dice as key elements become very important in terms of general availability at low cost, high yield and quality level. Today, different materials, e.g. Au, Ni, AuSn, SnAg, SnAgCu, SnCu, etc., are used for flip chip interconnects and different bumping approaches are available. Electroplating is the technology of choice for high-yield wafer bumping for small bump sizes and pitches. Lead-free solder bumps require an increase in knowledge in the field of under bump metallization (UBM) and the interaction of bump and substrate metallization, the formation and growth of intermetallic compounds (IMCs) during liquid- and solid-phase reactions. Results of a new bi-layer UBM of Ni–Cu which is especially designed for small-sized lead-free solder bumps will be discussed.

Keywords: Packaging; Flip chip; Bumping; Electroplating

1. Introduction

Assembly and packaging technology continue to change rapidly. In the last decade packaging has changed from simple single-die packaging to a complex system integration technology which represents an integral prerequisite for the manufacturing of new electronic products. Assembly and packaging needs are driven by market application requirements as well as silicon technology. Cost will drive technology trade-offs for all market segments. System in Package (SiP) technology has rapidly evolved from specialty technology used in a very narrow set of markets to a broad market base. The primary driver for SiP technology has been the need for more compact, more highly integrated electronics.

Permanently growing integration density and increasing complexity of integrated circuits lead to further reduced I/O pitches. A general roadmap, forecasted by ITRS [1], of selected parameter for devices (memory, μP and ASICs) regarding I/O counts, pitch frequency and power dissipation is presented in Table 1.

The selection of the interconnection technology for a specific application depends on topological, electrical and thermal considerations as well as reliability requirements, manufacturing and testing issues. The application of chip and wire bonding, which is the most commonly used interconnection technology today, is limited in terms of high I/O number, pad configurations and smallest pitches.

Flip chip (FC) technology offers several advantages especially for high dense interconnects because the whole chip surface may be used for a large number of I/O pads in area array configuration. Shortest interconnection lengths result in excellent electrical performance of interconnects as well.

2. Flip chip and bumping technologies

FC technology in contrast to chip and wire needs an additional process on wafer and/or substrate level—the bumping [3–5]. Depending on the selected joining process different bump configurations are used (Fig. 1). An overview about currently used bump metallization for different applications is given in Table 2.

For the metallization of the I/O pads, different bumping techniques have been developed. The most important are evaporation, electroplating, mechanical stud bumping and solder paste printing on wettable metallization like Ni/Au, as well as solder dispensing, immersion and solder transfer

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Table 1
Forecasted evolution of packaging parameter [1]

Year of prodution technology	2004	2007	2010	2013	2016
Technology node	hp90	hp65	hp45	hp32	hp22
Chip pad pitch (μm)					
Wire bond–ball	40	30	25	25	25
Wire bond–wedge	30	25	20	20	20
Area array flip clip (cost performance, high performance)	150	120	100	90	80
Peripheral flip chip (hand held, low cost, harsh)	60	30	20	20	15
Package pincount maximum					
Low cost	122–500	160–660	208–777	270–1011	351–1314
Cost performance (microprocessor/controller)	500–1600	600–2140	780–2782	1014–3616	1318–4702
High performance (microprocessor/controller)	3000	4000	4009	5335	7042
Harsh	500	660	642	812	1074
Chip frequency (MHz)					
Chip to board (off-chip) speed (high performance, for peripheral buses)	2500	4883	9536	48626	36379
On-chip (high performance)	3990	6740	12,000	19,000	29,000
Allowed maximum power (W)					
High performance with heatsink	158	189	218	251	288
Cost performance	84	104	120	138	158
Battery—(low cost/hand-held)	2.2	2.5	2.8	3.0	3.0

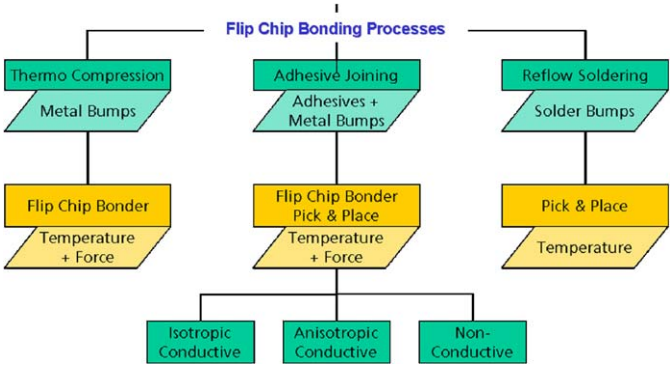

Fig. 1. Overview of FC approaches.

techniques. Each technique meets different requirement in terms of bump sizes, pitches, metallization, etc. Solder paste printing meets the requirement regarding low cost but this process is limited to minimal bump pitches of 150 μm today.

Wafer bumping by electroplating however, has the largest potential for realizing highest I/O densities with a pitch range from 200 to 25 μm. It is particularly suited for high volume production of bumped wafers at a high-quality standard. As the value of wafers increases, the relatively high processing costs are less and less perceptible.

The realization of bumps using electroplating can be divided into fundamental process steps, which are sputtering of the plating base, photoresist patterning, electroplating, differential etching, and, if required, a final solder reflow as shown in Fig. 2.

The selection of the suited bump metal and under bump metallization (UBM) depends mainly on the assembly process, the allowed joining temperature, the melting point of the solder, the integrity of the interfaces between the bump and the adjoining bond pad metallization, the bumping process compatibility and reliability requirements.

To preserve the structural integrity of all assembly parts, the temperature hierarchy in the package processing must be taken into consideration as well. All bump variations listed above are well established on 4″–8″ wafers at Fraunhofer IZM and available for specific customer requests.

3. Bumping process by electroplating

Typically, circuit device wafers have aluminum alloy pads and an inorganic (e.g. SiO_2, Si_3N_4, SiON) or organic passivation opened over the pads. InP or GaAs semiconductors for photonic and RF applications are using gold pads.

By an initial sputter-etching step, the wafer surface is cleaned of contamination and metal oxides. After back-sputtering an adhesion layer of Ti:W(N) with a thickness of 100–230 nm is sputtered on the whole wafer, followed by a second layer of either 300 nm Cu or 200 nm Au as a plating base. The specific addition of nitrogen (N_2) during deposit of Ti (5 wt%) W (95 wt%) enhances the diffusion-barrier property. A Ti:W(N)/Au bump structure on aluminum pads has shown no degradation after annealing at 400 °C (1 h). With optimized sputter conditions, a low-stress deposition and a good homogeneity of layer thickness are achieved without any damage of CMOS structures [2].

Spin coating is used to deposit the high-viscous photoresist onto the wafer in the desired layer thickness.