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DEPFET sensor design using an experimental 3d device simulator

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Abstract

A DEPFET sensor array element with rectangularly shaped channel geometry is simulated and optimized using an experimental three-dimensional (3d) device simulator. Due to the relatively large detector volume, the highly refined discretization necessary in MOS channels and the existence of floating potential regions within the DEPFET, the simulation is challenging especially in three dimensions. The results give valuable insight into all operation stages. Charge collection is in the focus here but also Read and Clear operation of the DEPFET are considered in order to evaluate the response of the device to a signal charge. The results are used to design the next DEPFET prototypes for ILC. The numerical features of the experimental 3d code are briefly discussed.

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Keywords: DEPFET; Active pixel sensor; Vertex detector; Linear collider; High-energy physics

1. Introduction

The DEPleted Field Effect Transistor structure, abbreviated DEPFET, provides detection and amplification properties jointly [1]. A MOS or junction field effect transistor is integrated onto a high-ohmic detector substrate. By means of sidewards depletion and an *n*-implant, a potential minimum for electrons is created underneath the transistor channel. This acts as an Internal Gate of the transistor. A particle entering the detector creates electron–hole pairs in the fully depleted silicon bulk. While the holes drift into the rear contact, the electrons are collected in the Internal Gate where they are stored. The signal charge leads to a change in the potential of the Internal Gate, resulting in a modulation of the channel current of the transistor. A more detailed description of the DEPFET structure and its operation can be found in Refs. [1,2]. The simultaneous detection and amplification feature makes DEPFET pixel detectors very attractive for low noise applications [3,4]. Due to its high signal to noise ratio at very low power consumption, the DEPFET can also be used on very thin detector substrates, for instance as a vertex detector for the International Linear Collider (ILC) [5]. Based on these inherent features, detector developments for X-ray spectroscopy [4] and for particle tracking [6–8] have been started. For space applications the minimum pixel size is defined by imaging properties of the X-ray mirrors. Rather relaxed pixel sizes of about 75 μm or larger can be chosen ensuring a large fraction of events with complete charge collection in one pixel and high-energy resolution. DEPFET pixel of this area can be designed with a closed annular channel geometry [4]. For the vertex detector at ILC much smaller pixel sizes in the range of 20–30 μm will be needed in order to meet the required point resolution of better than 5 μm [9]. An open rectangular pixel geometry must be used for layouts of this packaging density. In contrast to standard MOS transistors which are fabricated on low ohmic substrates, the DEPFET contains floating potential regions especially in the clear and insulation regions. This leads to complicated surface potential distributions which influence the movement of the carriers

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generated in the detector bulk. In this paper the emphasis is placed on the understanding and improvement of the charge collection process.

2. DEPFET pixel layout for an ILC vertex detector

Figs. 1 and 2 show the circuit diagram and the layout of a double pixel as arranged in an ILC prototype matrix, respectively. Two DEPFET rows are addressed by one set of control lines for the (External) Gates and the Clears of the double row. In this way, one degree of parallelization is implemented into the matrix layout. By bisection of the control lines the required row clock rate is reduced by a factor of two. The number of read out channels doubles of course. Another advantage of a double row addressing is its very compact layout. Each Drain, Source and Clear region can be shared by two neighboring cells. This symmetry results in an irreducible cell shown in Fig. 2 with Neumann boundary conditions.

In contrast to closed (annular) channel devices the open (rectangular) channel DEPFET needs a lateral insulation structure to suppress any parasitic lateral currents flowing from Source to Drain. This task is provided by the first poly silicon layer called Clear Gate which simultaneously defines the potential barrier between the Internal Gate and the Clear region as illustrated in the cross section through the Clear–Clear Gate–Internal Gate in Fig. 3. The DEPFET technology available at the MPI Semiconductor Laboratory in Munich is based on direct writing laser photolithography and conventional proximity exposure. Both methods allow the fabrication of wafer scale (150 mm) detector devices without chip stitching. Since the minimum feature size is about 2 μm, the size of crucial defects is in the same order of magnitude. This leads compared with submicron ULSI technologies to a higher fabrication yield for a given defect density and distribution what is even for the production of very large detectors very important. Nevertheless, the package density is limited by the minimum feature size. Hence smaller, simpler pixels are a design goal. As shown in Ref. [10], it is possible to keep the potential of the Clear Gate at a fixed value during all operation phases. Using this feature reduces the pixel size and the number of row control lines from three to two. It eliminates one of the two control chips (Switcher). The reduction of control and connection effort corresponds to less scattering material and is important for sensor applications in vertex detectors.

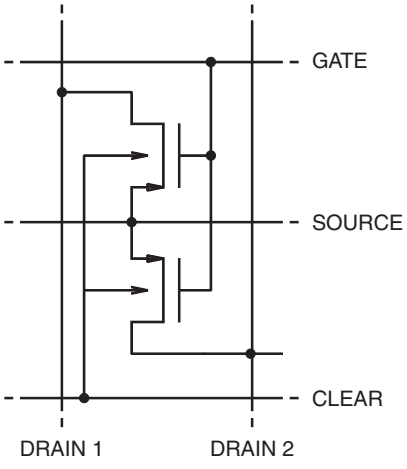

Fig. 1. Circuit scheme of an element of an ILC prototype array. Two DEPFET rows are addressed by one set of horizontal control lines.

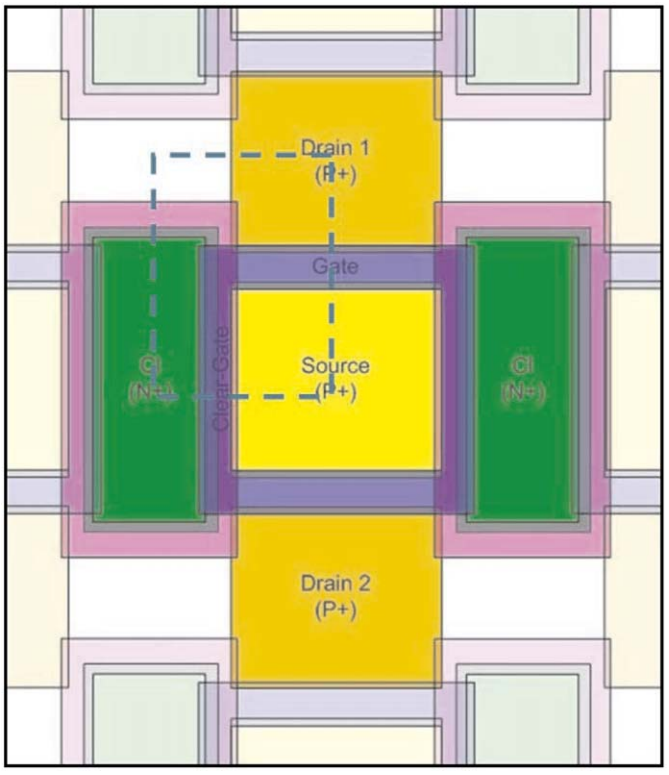

Fig. 2. Layout of a double cell used for the ILC prototype array. The dashed line marks the simulated region (Cl = Clear).

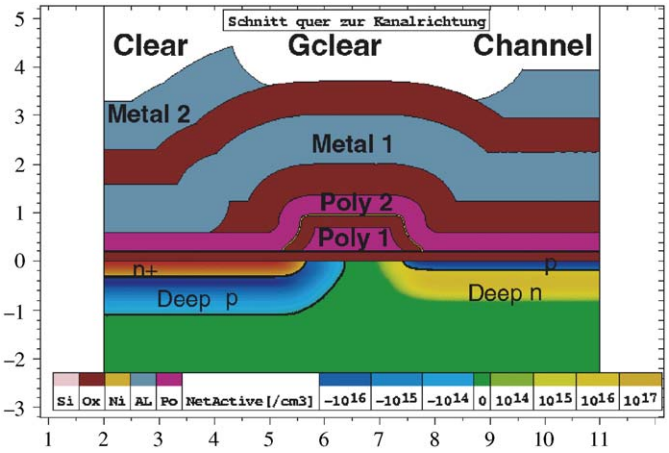

Fig. 3. Cross section through the Clear–Clear Gate–Internal Gate simulated with DIOS ISE-TCAD [11] (x and y scales in μm).