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Design criteria for low noise front-end electronics in the 0.13 μm CMOS generation

Valerio Re[a,c,*], Massimo Manghisoni[a,c], Lodovico Ratti[b,c], Valeria Speziali[b,c], Gianluca Traversi[a,c]

[a]*Dipartimento di Ingegneria Industriale, Università di Bergamo, Viale Marconi, 5, 24044 Dalmine, Italy*
[b]*Dipartimento di Elettronica, Università di Pavia, Via Ferrata, 1, 27100 Pavia, Italy*
[c]*INFN, Sezione di Pavia, Via Bassi, 6, 27100 Pavia, Italy*

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Abstract

The goal of this work is to provide an extensive analysis of the noise performances which can be attained by detector front-end integrated circuits in the 0.13 μm CMOS node. To estimate the noise limits of a front-end system in this CMOS generation, the paper presents the results of measurements carried out on NMOS and PMOS devices fabricated in a commercial process. Parameters extracted from experimental data are used to define design criteria for noise optimization in the perspective of future experimental environments (SLHC, ILC, Super B-Factory).

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1. Introduction

This paper presents a study of the performances achievable with integrated circuits for detector readout designed in the 0.13 μm CMOS generation. Microelectronic technologies are quickly evolving and scaling to feature sizes which are already in the 100 nm range. Presently, the question is if it will be possible to achieve low noise performances in future experimental environments going beyond the 0.25 μm CMOS technology, which is widely used nowadays for a large family of readout systems [1–4]. The goal of this work is to answer this question by discussing the results of the experimental characterization of a commercial 0.13 μm CMOS process by STMicroelectronics. Low-noise design in deep submicron CMOS requires to monitor the impact of channel length and oxide thickness scaling on white and $1/f$ noise parameters of MOSFET devices. Because of power dissipation constraints, the focus is mostly on low current density (that is, weak and moderate inversion) operating regions. In the perspective of experiments at the next collider generation (SLHC, ILC, Super B-Factory), noise performances can be very critical where a very short signal shaping time is required because of high event rate, or where a thin silicon detector (100 μm or less) is mandatory for material minimization or radiation hardness.

2. Noise characterization

2.1. Technology and test devices

The MOSFETs studied in this work belong to the 0.13 μm CMOS process by STMicroelectronics (HCMOS9). We tested standard devices in this technology, with an oxide thickness t_{OX} of 2.4 nm, a gate capacitance per unit area C_{OX} of about 14.8 fF/μm^2 and a maximum

*Corresponding author. Dipartimento di Ingegneria Industriale, Università di Bergamo, Viale Marconi, 5, 24044 Dalmine, Italy. Tel.: +39 035 2052311; fax: +39 035 562779.
E-mail address: valerio.re@unibg.it (V. Re).

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supply voltage V_{DD} of 1.2 V. The devices are based on a standard open-structure interdigitated layout.

2.2. Noise equations and device operating region

In a CMOS analog channel for detector signal processing, noise is usually determined by the properties of the preamplifier input device, which can be expressed in terms of the gate-referred noise voltage spectrum $S_e(f)$

$$S_e^2(f) = S_W^2 + \frac{K_f}{C_i}\frac{1}{f^{\alpha_f}}. \quad (1)$$

The first term in Eq. (1) is determined by channel thermal noise and by noise in parasitic gate and substrate resistors. The contributions from these resistors usually have a minor impact in the low current density operating region [5]. The second term is given by $1/f$ noise in the channel current. K_f is an intrinsic process parameter for $1/f$ noise and C_i is the input capacitance, $C_i = C_{OX}WL$. W is the gate width, L is the gate length. The exponent α_f determines the slope of this low-frequency noise term.

The white noise voltage spectrum S_W can be expressed in all inversion regions [3,6] by the relationship

$$S_W^2 = 4kT\frac{\Gamma}{g_m} \quad (2)$$

where g_m is the transconductance, k is the Boltzmann's constant and T is the absolute temperature. The value of the coefficient Γ is determined by the device operating region and takes into account possible excess noise, which in submicron devices may be given by short channel effects.

In mixed-signal detector readout systems, power dissipation constraints set an upper limit on the drain current I_D in the preamplifier input device. In most cases, this means that the device is operating close to the weak inversion region, where the transconductance is

$$g_m = \frac{I_D}{nV_T}. \quad (3)$$

In Eq. (3), $V_T = kT/q$ is the thermal voltage and the coefficient n is proportional to the inverse of the subthreshold slope of I_D as a function of the gate to source voltage V_{GS}. It is possible to define a characteristic normalized drain current I_Z^* which sets the boundary between weak and strong inversion [7,8]

$$I_Z^* = 2\mu C_{OX} n V_T^2. \quad (4)$$

At $I_D L/W = I_Z^*$, the device is operating in moderate inversion. I_Z^* is expected to be larger in NMOSFETs (larger carrier mobility μ) and in devices fabricated in processes with smaller minimum feature size (larger C_{OX}). This means that the weak and moderate inversion regions extend to higher normalized drain currents in the most advanced CMOS generations. This is supported by the experimental results shown in Figs. 1 and 2. Fig. 1 is relevant to devices in the 0.13 μm CMOS technology, and shows the larger extension of the weak inversion region

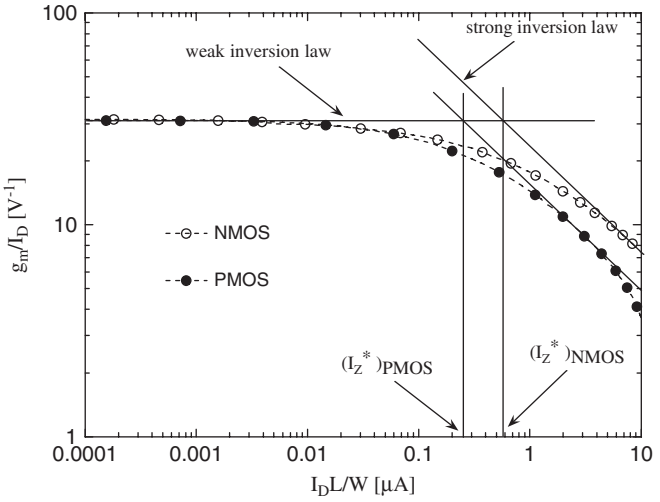

Fig. 1. Transconductance-to-drain current ratio as a function of the normalized drain current for devices in the 0.13 μm process by STMicroelectronics measured at a drain-to-source voltage $|V_{DS}| = 0.6$ V. For NMOS (white dots) and PMOS (black dots) $W/L = 1000/0.2$.

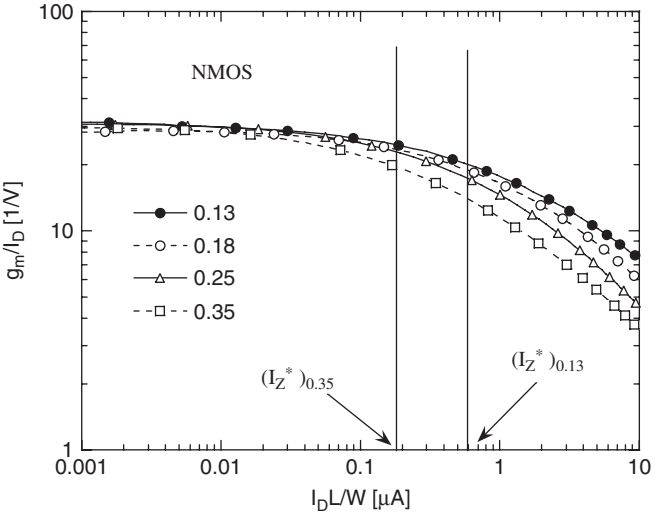

Fig. 2. Transconductance-to-drain current ratio as a function of the normalized drain current for NMOS devices in CMOS processes from the 0.35 μm node to the 0.13 μm node. The plot reports data relevant to devices in the 0.35, 0.25 and 0.18 μm processes manufactured by TSMC and in the 0.13 μm process by STMicroelectronics.

(where the ratio g_m/I_D is constant and independent of the drain current and of the device gate width and length) in NMOSFETs with respect to PMOSFETs. The plot also shows that at large drain current density the devices enter the strong inversion region, where g_m has a square root dependence on I_D. Fig. 2 compares the behavior of g_m/I_D in NMOSFETs belonging to four CMOS nodes, from 0.35 to 0.13 μm. The plot shows that an implication of CMOS scaling is that the parameters of devices operating in low power systems closely match the predictions of weak inversion laws such as Eq. (3) in a wider region in more scaled processes.