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A DEPFET pixel matrix system for the ILC vertex detector

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Abstract

The DEPFET detector offers radiation detection and amplification jointly by embedding a field effect transistor into fully depleted silicon. Due to the excellent noise performance (ENC = 2.2 e^- for single pixel at room temperature and 6 μs shaping time) and the high spatial resolution of the device (4.3 μm at 22 keV using $50 \times 50\,\mu m^2$ pixels), the DEPFET concept is attractive for X-ray astronomy, for biomedical application and for tracking in particle physics. For the vertex detector of a future TeV-scale linear collider, like the proposed ILC (International Linear Collider), a highly granulated pixel system operated row-wise with line rates of 20 MHz at a noise level below 100 e^- is needed. Addressing these requirements, improved DEPFET sensors with $22 \times 36\,\mu m^2$ pixel size have been fabricated. A prototype system has been developed that uses dedicated chips for steering and readout of a 64×128 DEPFET pixel matrix. Due to the current based readout mode provided by the readout chip, a thousand times faster matrix operation than achieved so far is possible. The performance of the single components of the system will be summarized and first results obtained with the entire system will be presented.

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1. Introduction

The ILC offers a large variety of precision measurements complementary to the discovery potential of the Large Hadron Collider (LHC). To fully exploit this physics potential, a vertex detector of unprecedented performance is needed. While state of the art pixel systems like hybrid pixels or conventional CCDs can fulfill the requirements of present experiments, new pixel developments are necessary for future linear colliders, where thin detectors with less than 0.1% X_0 per layer, lowest power consumption and small pixel sizes of about $25 \times 25\,\mu m^2$ are needed [1].

Since the accelerating system of the ILC has been decided to be a superconducting one, the timing structure of the bunch will probably be similar to the TESLA proposal. Due to the prominent pair production background near the interaction point (80 hits per mm^2 and bunch train at $r = 15$ mm) a multiple readout (10–30 times) of the vertex detector during the bunch train is inevitable to keep the occupancy at a reasonable level. Reading out a whole DEPFET pixel based vertex detector containing almost 10^9 pixels in 50 μs, line rates of 20 MHz in the ladders are required. At the same time, a noise figure below ENC = 100 e^- is desirable. Facing these challenging requirements, the DEPFET detector is a promising approach for a future micro vertex detector.

2. The DEPFET concept for a micro vertex detector

The DEPFET pixel detector [2] combines in-pixel amplification with particle detection by integrating a field-effect-transistor in a fully depleted silicon sensor. The high resistivity sensor material is depleted by means of sidewards depletion, forming a potential minimum for

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electrons underneath the transistor channel, the internal gate. Electrons created by impinging particles are accumulated in the internal gate, insensitive to outer electromagnetic disturbances and modulate the transistor current. In this context, the figure of merit of the DEPFET is the amplification of the internal gate, $g_q = \mathrm{d}I/\mathrm{d}Q$, where $\mathrm{d}I$ is the change of the device current and $\mathrm{d}Q$ is the accumulated charge in the internal gate. Present devices show an internal amplification of about $280\,\mathrm{pA/e^-}$, whereas more advanced pixel designs propose an amplification of up to $1\,\mathrm{nA/e^-}$ [3]. As the charge is not removed from the internal gate by probing the transistor current, DEPFET pixel need an external reset mechanism, also known as the clearing of the internal gate. The reliability of the clear mechanism has already been demonstrated in [4] as it is essential for providing a stable pedestal reference in an ILC operation mode.

Pixel in a matrix are addressed like in a RAM structure: One row is selected after each other and the pixel currents are probed column wise at the bottom of a matrix. Such a row-wise operation mode features a very low power consumption being a crucial criteria of the cooling scheme at a future linear collider.

Due to the internal amplification and due to the possibility of making small pixel the particular attributes of the DEPFETs are an excellent noise performance and a high spatial resolution at the same time [5]. For the ILC vertex detector, the DEPFET detector offers the possibility to fabricate 50 μm thin devices [6] which still offer an excellent signal to noise ratio of about $S/N \approx 40$.

3. The ILC DEPFET-System

A photograph of the ILC DEPFET-System is shown in Fig. 1. It consists of two major parts, a sensor PCB (left) and a stack of DAQ-boards (right), both connected by a ribbon cable to maintain higher flexibility. The DAQ-boards provide an USB based communication with a PC, configure the steering and readout chips and digitize and store the analog data. The sensor PCB hosts the DEPFET pixel matrix driven by two steering chips SWITCHER II for row selection and reset. The columns of the matrix are read out in parallel at the bottom by the CURO II chip (see Fig. 2).

Since a fast readout is one of the crucial points of the ILC-system a completely current based approach has been chosen, the CURO (CUrrent Read Out) Architecture. It is well suited to the signal of the DEPFET, which is intrinsically a current. Upon the many advantages of the current mode signal treatment, the most important ones are: a high dynamic range can be preserved while supply voltages decrease in modern chip technologies, and, a very convenient and accurate subtraction of two currents is possible, like it is needed for a pedestal subtraction.

The readout principle of the CURO-Architecture is illustrated in Fig. 3. The input stage is realized by a regulated cascode providing a low input impedance for the DEPFET current. The readout of one matrix row is performed as follows: After one row in the sensor matrix has been selected for readout, the signal current of the pixel superimposed on a pedestal current $I_{\mathrm{sig}} + I_{\mathrm{ped}}$ is stored in a current memory cell. A detailed description of the current memory cell can be found in [7]. The row is then reset and the remaining pedestal current provided by the sensor I_{ped} is automatically subtracted at the memory cell. The resulting signal current I_{sig} is stored alternately in two buffer cells. In the succeeding cycle the front end is ready again for the input current of the next DEPFET row. Meanwhile, the signal current in the buffer cell is compared with a programmable threshold and the digital result is stored together with the analog value in a small mixed signal FIFO. Simulations show that a FIFO depth of 4

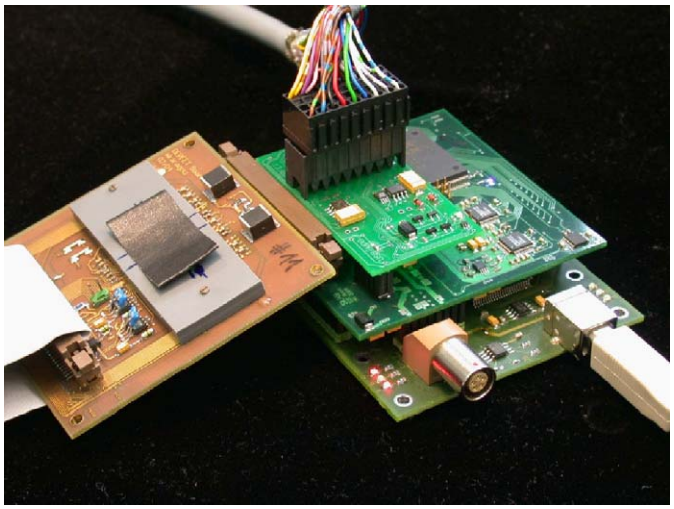

Fig. 1. Photograph of the ILC DEPFET-System. The sensor matrix and the chip assembly are protected by a plastic cap on the sensor PCB.

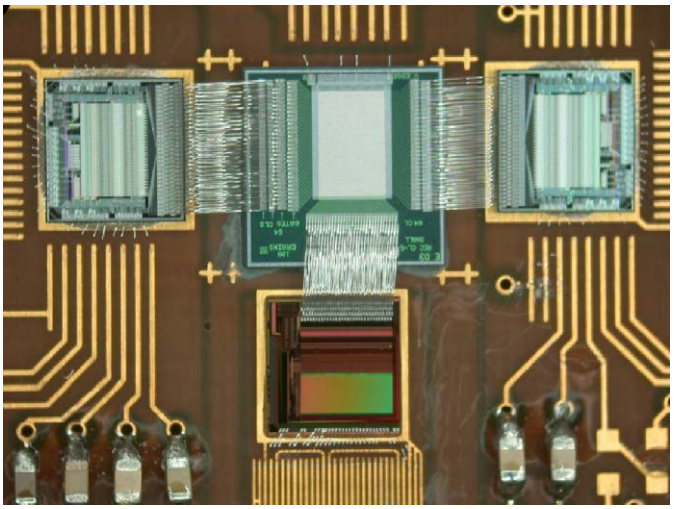

Fig. 2. Micro photograph (area shown: $23 \times 16\,\mathrm{mm}^2$) of the chip arrangement on the sensor PCB, a 64×128 pixel DEPFET-Matrix (middle), two steering chips SWITCHER II (left & right) and the readout chip CURO II (bottom).