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# Technology development for SOI monolithic pixel detectors

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**Abstract**

A monolithic detector of ionizing radiation has been manufactured using silicon on insulator (SOI) wafers with a high-resistivity substrate. In our paper the integration of a standard 3 μm CMOS technology, originally designed for bulk devices, with fabrication of pixels in the bottom wafer of a SOI substrate is described. Both technological sequences have been merged minimizing thermal budget and providing suitable properties of all the technological layers. The achieved performance proves that fully depleted monolithic active pixel matrix might be a viable option for a wide spectrum of future applications.


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*Keywords:* Silicon radiation detectors; Position pixel detector; Silicon on insulator technology

## 1. Introduction

A silicon on insulator (SOI) wafer consists of a monocrystalline Si film (device layer) over an insulating layer of $SiO_2$ (buried oxide—BOX) on a Si substrate (handle wafer). In the standard SOI technologies, the handle wafer serves as a mechanical support for the device layer with the integrated circuits. In our detector instead (see Fig. 1), the high-resistivity handle wafer is used for the fabrication of the sensor (a matrix of fully depleted diodes) monolithically coupled to the read-out electronics integrated in the device layer.

That idea was published more than 10 years ago [1] and then a prototype was produced [2]. In this approach, a pixel detector with an electrostatic shield structure formed inside each pixel area was fabricated in the handle wafer and the mating read-out electronics in the device layer of a bond-and-etch-back SOI (BESOI) wafer. The shield structure and the pixel junctions were manufactured prior to the SOI wafer bonding process. Due to errors in the process flow this approach was unsuccessful.

Next, a SOI active pixel image sensor (for visible light) with the photodiodes fabricated in the handle wafer was developed [3]. The sensor was based on a separation by implantation of oxygen (SIMOX) low-resistivity p-type wafer. Therefore the detector could not provide advantages of the fully depleted one.

Recently, a similar device has been fabricated at JPL using Unibond (SmartCut) SOI wafers with low handle wafer doping [4] but the device geometry did not provide full depletion (being optimized for visible light imaging). The read-out electronics has been manufactured with conventional partially depleted SOI technology.

## 2. SUCIMA SOI sensor

The development of sensors for fast imagers specified for medical applications was one of the major goals of the SUCIMA [5] project. The use of a SOI substrate with the high-resistivity fully depleted handle wafer enhances significantly the signal-to-noise ratio as compared to bulk CMOS imagers or SOI sensors on a low-resistivity

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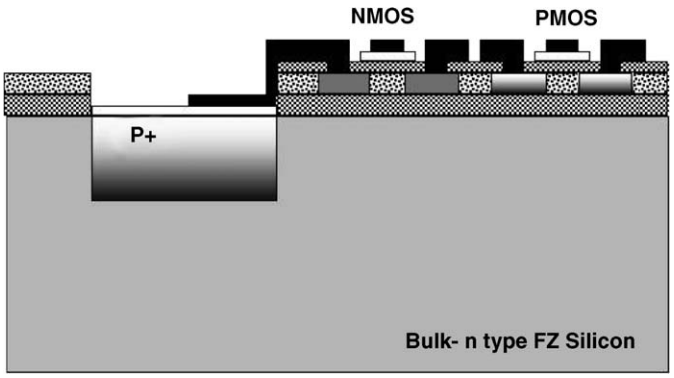


Fig. 1. The idea of the fully depleted active pixel sensor manufactured in SOI technology.

substrate. Also the sensitivity to soft X-rays benefits from the typical thickness of the fully depleted detector. In our device, the active volume can be also reached by back-illuminating the sensor. The details on the device may be found in Ref. [6].

### 2.1. Choice of substrate

The first decision concerned the kind of SOI wafers. Since the device layer should be of low-resistivity, while the handle wafer—of high-resistivity, the SIMOX wafers were excluded. Standard BESOI wafers are difficult to accept because the thickness variation of the device layer results in variation of the threshold voltage of MOS transistors. There are several techniques offering extremely low variation of the thickness like SmartCut (SOITEC) or ELTRAN (Canon) but they are hardly available for small-volume non-typical orders. Finally, the prototype was manufactured using BESOI wafers from Analog Devices (AD).

The 4″ SOI substrates consisted of FZ, ⟨100⟩, n-type, 4 kΩ cm, 400 μm handle wafer; 1 μm BOX; and 2 μm, *Cz*, ⟨100⟩, 9–13 Ω cm, p-type device layer (later overcompensated). The device layer thickness of 2 μm (0.25 μm standard deviation) has been chosen taking into account the minimum device layer size available at the AD and compatibility with the standard Unibond (SmartCut) test wafers used for validation of the CMOS technology. The relatively thick device layer allowed not only the use of the modified bulk technology, but it was also desirable to decouple effectively the read-out circuitry from the sensor.

### 2.2. Strategic decisions

The DC coupling between detecting diodes and read-out circuitries has been chosen since it offers much shorter technological sequence and simpler layout than the AC solution. The minimum cross-talk has been achieved by careful setting of potentials beneath MOS transistors using a fine grid of ohmic contacts. The full process flow accounted for the following issues:

- long lasting high-temperature processes have been done before making pixel openings in the BOX,
- the thermal budget of the whole process sequence has been minimized,
- the process sequence determining the pixel cavity shape assured the continuity of the metal paths,
- the shallow backside contact has been designed for a purpose of low-energy beta detection.

### 2.3. Test structure

The dedicated test structure SUCIMA1 shown in Fig. 2 has been designed, fabricated, and tested for the technological and the functional assessments. There are modules for tests of conducting paths, modules for extraction of parameters of layers and semiconductor devices. Moreover there are simple digital and analog cells and cells for mismatch and reliability studies (current mirrors).

Several small area detectors ($8 \times 8$ pixel matrices with 130 μm pitch) have been implemented on the chip, featuring either an access to the input node of the cell for charge injection or a connection to the pixel junction.

### 2.4. Technology choice and its verification

It should be pointed out that in our approach the CMOS circuitry, although it was made in a SOI device layer, has been based on bulk (non-SOI) transistors. The above mentioned test structures have been used to characterize and to tune the technology. The doping profiles for the MOS transistors on thin SOI substrates are different from those manufactured in the bulk. Thus, adapting a bulk technology to the SOI application required matching of technological parameters to get required MOSFETs parameters.

The pixel quality has been assessed by measurements of reverse characteristics of the test pixel junctions. In

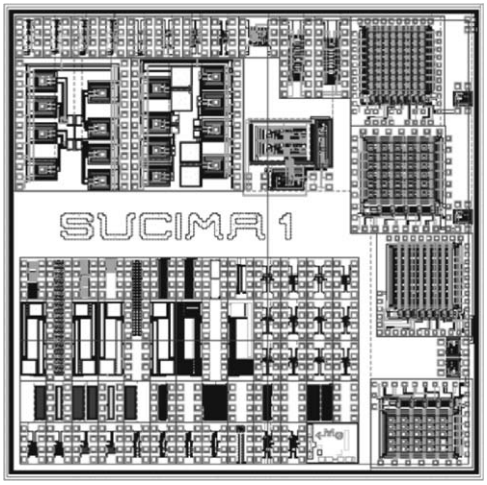


Fig 2. The view of the test structure SUCIMA 1.