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Development of an electronic board for a neutrino telescope project

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Abstract

The NEMO (NEutrino Mediterranean Observatory) collaboration is involved in research and development for the construction of an underwater km^3 scale Cherenkov neutrino detector. The detector will consist of about four thousands of optical modules that interface with coaxial cables to electronics cards. The detector is connected to the shore by an electro-optical cable for data transmission and power supply. The board also provides signal synchronization, filtering, data compression and packing. We describe the details of this electronic control part, which has been developed using commercial components and the very high-speed, Hardware Description Language (VHDL). The design was implemented on a programmable device. A test-bench system was also designed using a PC-based acquisition board running on the National Instrument LabVIEW environment.

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1. Introduction

Over the last decades, the observation of cosmic rays of ultra high-energy (UHE), even with energies greater than 10^{20} eV, has attracted the attention of the scientific community [1]. UHE sources of cosmic rays may yield an associated flux of high-energy neutrinos [2]. In 1960, Markov [3] proposed using seawater or underground detectors as huge targets to detect UHE neutrinos via charged current weak interactions in the water or in the rock [4,5]. The outgoing leptons (muons) carry a considerable part of the neutrino energy and preserve the neutrino direction, propagating in seawater for several km [6,7]. In other words, the identification of the muon track allows the reconstruction of the neutrino direction.

High-energy muons, moving at high speed in water produce a trail of Cherenkov light [8] which may be detected by a 3-dimensional lattice of photo-multiplier tubes (PMT). Only upward-going muons are considered since they result only from neutrino reactions in the earth, below the detector [9]. New calculations indicate that a detector as large as 1 km^3 equipped with several thousand PMTs may be capable of yielding significant results. In view of the practical limitations imposed by the size of the detector, the planned neutrino detector medium is the deep-sea water [10,11]. The water above the sensors is necessary to shield the detector volume from undesired cosmic radiation. The NEMO proposal is a feasibility study of a km^3 underwater telescope for high-energy (greater than 10^{12} eV) astrophysical neutrinos. It may be located in the Mediterranean Sea about 80 km from Capo Passero (Sicily) [12]. A single optical module includes a PMT for Cherenkov light detection and an electronic board for data acquisition and transmission. Similar modules have been applied successfully in previous neutrino detectors [13]. The main features of the modules are already defined. The PMT must deal with an average event rate of 30–60 k event/s depending on a predefined threshold.

The detector will consist of a hierarchical structure of optical modules, arms and towers [14]. The signals of the

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PMTs are collected via 1st level concentrators. Then, the data coming from the 1st level concentrators are grouped via 2nd level concentrators. The whole system exchanges signals from the shore to the optical modules and from the optical modules to the control station through a single main backbone cable. The effective volume of the detector is slightly smaller than its physical volume which is of the order of 1 km^3.

2. Board description

This paper describes the design of a prototype of the electronic board that may control the optical module and the related front-end acquisition system of the NEMO project. A simulation and data-logging system was designed to test the board. The system is an evolution of a previous version of the board [15]. For testing it uses a Field Programmable Gate Array (FPGA); if replaced by a dedicated Application Specific Integrated Circuit (ASIC), the power consumption could be much reduced. Other components, such as the trigger, the analog memories and the Analog to Digital Converter (ADC), are mentioned with their interfaces. Fig. 1 shows the electronic control board that has already been constructed and tested.

When the tube inside each optical module produces a signal, a trigger element starts the acquisition process, and via the programmable device triggers the analog memories (now off-board) to begin the sampling process of the detected charge (Lo Presti, priv. commun.). Once the memory block is full, the control unit starts the conversion of the acquired dataset via the ADC. Two analog memories are configured in a double buffer structure, thus limiting dead time. The digital dataset enters the FPGA where it is packed and transmitted to the 1st level concentrator. This is done via an encoded serial stream at a 5 Mbit/s. The data transmission protocol includes start and end codes for the transmission of single packets. These codes contain event and time information (Ameli, priv. commun.).

2.1. Functional units

Fig. 1 shows the board with its electronic blocks. The shaded blocks can be mounted separately to test the FPGA alone, while the dashed blocks are mutually exclusive with other parts. Below, the mentioned blocks are summarized with a brief functional description; their names refer to the notation of Fig. 1.

FPGA	it is a synchronization component and a main control unit
ADC	it reads the analog memories at a rate of 10 MHz. This component can be bypassed by providing a 10-bit digital data (shape$\langle 9{:}0 \rangle$ in Fig. 1)
Phase Locked Loop (PLL)	it locks and multiplies the global clock signal to get to the 20 MHz master clock signal Mclk. It needs a circuit (Filter & Conditioning in Fig. 1) to extract the 1 MHz carrier from the cable
20 MHz oscillator	it is a mutually exclusive device with the previous PLL
Transformer 1:1	it is a transmitter–receiver component used to decouple the cable from the on-board signals
Conditioning & cable driver	it drives and extracts the signals from the cable and
Filter	it extracts the power supply. This can be bypassed via two regulators (PCB Power Supply in Fig. 1).

The above components were mounted on the board. By contrast, the following must be mounted on external cards provided by the NEMO collaboration:

- Analog memories: they sample at 200 MS/s the PMT signals and work as first-in-first-out analog devices; and
- Trigger: it starts basically the data acquisition.

The board is fully line-powered through the coaxial cable.

To date, this board has been developed as a prototype without taking into account the power consumption. Due to the large number of optical modules the global power consumption will be defined in the future when the whole project will be fully designed in more detail.

At the moment the main purpose of the board is to test the signal connections and the data transmission. The on-board control unit includes a sufficiently deep digital buffer that works as a queue-buffer for reading data from the ADC and writing the corresponding compressed and packed dataset on the serial out port of the board.

2.2. Data flow

The data transmission starts from 4 optical modules in a single tower beam. The data are collected via a 1st level concentrator and a tree-like structure applies up to the 3rd level concentrators that are connected to the shore. For the optical module viewpoint, the communication refers only to its 1st level concentrator. This latter device provides the optical modules with 3 specific things embedded into coaxial cables: the power supply, the slow-control signals and the clock. A rough estimation of the consumption of the proposed prototype is 1 W per board. In the case of low-power electronics this is estimated in only few hundreds of mW. The slow-control signals are a set of configuration instructions transmitted from the control station. The programmable device located on the board also decodes the slow-control signals. A 1 MHz clock signal enters all the optical modules continuously and this is the global synchronization signal. Since the slow-control signals and the clock run in the same direction, from the 1st level of concentrators to the optical modules, they are embedded into an auto-synchronous encoding. The 0–1