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Pathway to low-cost metallization of silicon solar cell through understanding of the silicon metal interface and plating chemistry

Abasifreke Ebong*

Energy Production and Infrastructure Center (EPIC), Department of Electrical and Computer Engineering, The University of North Carolina, 9201 University City Boulevard, Charlotte, NC 28223-0001, United States

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ABSTRACT

Metallization is crucial to silicon solar cell performance. It is the second most expensive process step in the fabrication of a solar cell. In order to reduce the cost of solar cell, the metallization cost has to be cut down by using less metal without compromising the efficiency. Screen-printing has been used in metallizing the commercial solar cell because of the high throughput and low cost at the expense of performance. However, because of the variability in the screen-printed gridlines, the amount of Ag metal used cannot be controlled. More so, the dependence of the contact resistance on doping necessitates the use of low sheet resistance emitters, which exacerbates losses in the blue response and hence the efficiency. To balance the contact resistance and improve blue response, several approaches have been undertaken including, use of Ag pastes incorporating nanoparticle glass frits that will not diffuse excessively into a lightly doped emitter, Ni plating on lightly doped emitter through SiNx dielectric plus NiSi formation followed by Cu and/or Ag plating, light induced plating (LIP) of Ag or Cu on fired through dielectric metal seed layers formed by aerosol or inkjet or screen-printing. All these approaches require excellent adhesion and gridline conductivity to minimize the total series resistance, which impedes the collection of electrons. This paper presents the issues and the pathway to achieving high efficiency using low cost metallization technology involving inkjet-printed Ag fine gridline having 38 μm width and 3 μm height fired through the SiNx followed by Ni and Cu plating. A comprehensive analysis of silicon/metal interface, using high precision microscopy, has shown that the investigated metallization technology is appropriate for the longevity of the device.

1. Introduction

Solar electricity is an attractive alternative to fossil fuel because it is benign to the environment. However, the cost of manufacturing the system, which converts sunlight into electricity, must be addressed. The traditional value chain for solar electricity is shown in Fig. 1, which encompasses polysilicon, wafering, cell fabrication, module fabrication, systems and grid integration. The cost of each chain must be controlled in order to decrease the total cost of manufacturing and hence the cost of solar electricity. The cost of polysilicon, for instance, has come down remarkably since 2010 and that has enabled the wafer cost to drop. However, cell fabrication cost must follow suit. The commercial cell uses screen-printing because of low-cost and high throughput. The efficiency on the other hand is lower than other non-commercial technologies. In, particular, the cost of silver used for metallizing the solar cell varies daily and ~120–140 mg of Ag is required per 6 in. wafer. This costly material needs to be replaced or reduced. That's why the two-step metallization of seed layer plus sintering and then plating is being investigated so that lower cost metals such as Ni and Cu can be used in place of Ag. This paper investigates a two-step metallization of solar cell involving printed seed layer followed by rapid thermal sintering and then Ni, Cu and Ag plating by light induced plating (LIP).

1.1. Light induced plating (LIP) of metal to sintered solar cell gridline

Mette et al. [1] first reported the use of LIP with screen printed solar cells showing ~0.3–0.4%, absolute, efficiency gain. In this report, the authors assumed the contact resistance was low so that the total series resistance of the cell was dominated by the gridline component. The authors concluded that the improvement observed in the fill factor was due to a decrease in the gridline resistance. However, the reported solar cell was fabricated on 55 Ω/sq emitter, which can be contacted without any contact resistance issues. Oberholtzer and Dube [2] reported cells fabricated on 75 Ω/sq emitter, which would have poor contact but with the application of LIP

* Tel.: +1 704 687 0307; fax: +1 704 687 4762.
E-mail addresses: aebong1@uncc.edu, abaebong@yahoo.com

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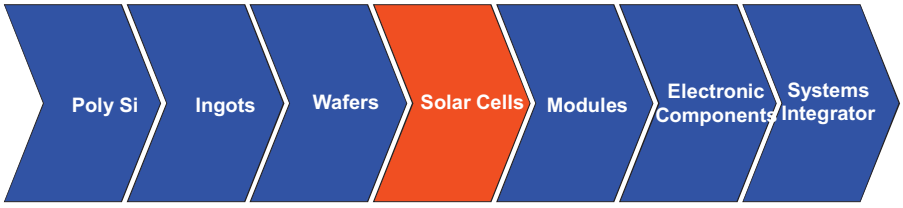

Fig. 1. The traditional value chain for solar electricity.

the fill factor improved by ~10%. To understand the effect of LIP on the series resistance and >75 Ω/sq emitter, Ebong et al. [3] dipped the screen-printed contact in LIP for 45 s and observed a fill factor improvement of ~10%. They concluded that the LIP chemistry etched the glass at the periphery of the gridline and improve the conduction of carriers through the contact. Thus, the improvement in fill factor was attributed to decrease contact and gridline resistances. That is, the excess glass at the edges of the finger is, first etched by the plating chemistry and then plate to fill the gaps after a long time in the plating solution. This action forms a low resistance path and increases the gridline conductivity to allow more current to pass through. In this case the amount of Ag required to obtain high quality contact is at least 140 mg per 6 in. wafer. This is equivalent to Ag cost of 14¢ per 6 in. wafer, assuming the price of Ag/kg is $1000 and corresponds to ¢3.1/Wp, if every 6 in. wafer produces 4.5 Wp. To reduce the cost of metallization of solar cell, alternative metal such as Ni and Cu should be used. The cost of Ni and Cu is very low and even if 140 mg of combined metal was deposited on 30 mg seed layer of Ag, the cost of metallization per wafer will still be <4¢/wafer. This means the cost of metallization of ~¢1.0/Wp is realizable.

Further investigation was done to fully understand if a short time LIP can decrease gridline resistance. It is well known that forming gas anneal (FGA) can improve the fill factor because the hydrogen from FGA can reduce the metal oxide to metal and increase the conductivity of the fired screen-printed gridline [1–3]. HF dip was also observed [4] to reduce the contact resistance but compromised adhesion. To understand these three phenomena and quantify the effect on contact and gridline resistances, samples were prepared for contact and gridline resistance measurements. In each case, the as fired gridline resistance was measured before subjecting the sample to HF, LIP or FGA, and then measured. Equally so to the samples prepared for the contact resistance measurements. Fig. 2a and b shows the results of the investigation. Fig. 2 shows the gridline resistance before and after gridline sintering and after HF, LIP and FGA. It is clear that the short time HF dip does not change the gridline resistance and this is true for LIP and FGA. Fig. 2b shows the contact resistance as each sample went through the different treatments. The contact resistance after the treatments drops by an order of magnitude. This confirms the reduction in series resistance and improvement in FF is due to the decrease in contact resistance by the LIP or HF or FGA.

Note that because the gridlines are thick, the HF and LIP can penetrate only ~10 μm [5] from the edges. Thus, in the case of two-step metallization, where the seed layer is only 3–5 μm thick, then the LIP chemistry would penetrate the entire contact region and decrease the contact resistance in the first few seconds and then plate to increase the gridline conductivity.

2. Experimental

Large area (243.4 cm^2) commercial Czochralsky (CZ) silicon wafers of 2–3.4 Ω cm resistivity having 180 μm thickness were textured, both sides, rinsed in dilute HCl before cleaning in H_2SO_4:H_2O_2:H_2O for 5 min, followed by a 3 min rinse in deionized (DI) water. A final dip in 10% HF for 2 min was performed, followed by a 30-s rinse in DI water. After the cleaning, the emitters were formed in conventional tube furnace using $POCl_3$ at a set temperature of 845 °C, which resulted in 100–110 Ω/sq emitters. Next edge isolation was performed. After the phosphorus glass removal and DI water rinse, a single layer low frequency PECVD SiN antireflection coating was deposited on the front at 400 °C. Next, Ag/Al stripes were printed on the back and dried at 200 °C followed by a screen-printed Al on the back side and dried at 200 °C. This was followed by front Ag seed layer (~3 μm thick) printing using digital inkjet printer. The drying step after the inkjet printing is avoided because the stage at which the wafer is placed is at >200 °C, therefore, the ink is dried as it is printed. Next, the samples were co-fired in the IR belt furnace after a controlled profile to ascertain the peak firing temperature, which ranged from 740 to 795 °C. This was followed by LIP plating of Ni/Cu and then Ag dip in the order 2.5/18/0.5 min, before light *I*–*V* measurements.

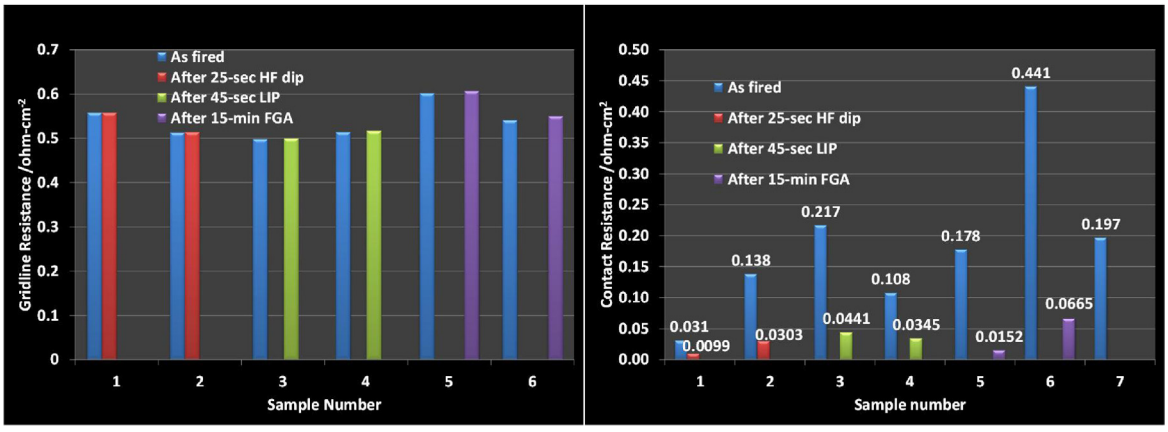

Fig. 2. (a) and (b) Effect of HF, LIP and FGA, respectively, on gridline and contact resistances of sintered Ag.