Physics Letters A 376 (2012) 957–962

Contents lists available at SciVerse ScienceDirect

Physics Letters A

www.elsevier.com/locate/pla

Noise-assisted morphing of memory and logic function

Vivek Kohar, Sudeshna Sinha *

Indian Institute of Science Education and Research (IISER) Mohali, Sector 81, SAS Nagar, Mohali 140 306, India

ARTICLE INFO

Article history:
Received 4 October 2011
Received in revised form 22 December 2011
Accepted 24 January 2012
Available online 28 January 2012
Communicated by A.R. Bishop

Keywords:
Stochastic resonance
Memory
Logic gates
Nonlinear circuits

ABSTRACT

We demonstrate how noise allows a bistable system to behave as a memory device, as well as a logic gate. Namely, in some optimal range of noise, the system can operate flexibly, both as a NAND/AND gate and a Set–Reset latch, by varying an asymmetrizing bias. Thus we show how this system implements memory, even for sub-threshold input signals, using noise constructively to store information. This can lead to the development of reconfigurable devices, that can switch efficiently between memory tasks and logic operations.

1. Introduction

While the number of transistors in an integrated circuit has approximately doubled every year in accordance with Moore's law, the rapid shrinking of computing platforms with smaller power supplies has brought with it problems of smaller noise margins and higher error rates. So wide ranging research efforts in recent years have focused on the issue of reliable operations in the presence of a noise floor [1].

In this context, recently it has been shown that a noisy nonlinear system, when driven by two square waves encoding two logical inputs, consistently goes to a state that mirrors a logical combination of the two inputs (such as AND/NAND and OR/NOR logic, cf. Table 1) in some optimal range of noise [2]. That is, the probability of getting the correct logical response increases to unity with increase in the intensity of noise and then decreases again when noise exceeds the optimal range. Further one can vary the threshold (or bias) and morph the output into different logical functions. This concept, named "Logical Stochastic Resonance" [2–9], helps one gain understanding of the counter-intuitive interplay between noise and nonlinearity [10]. Further, from the applied viewpoint, this idea can potentially lead to the design of flexible logic gates with enhanced performance in noisy environments [2–9].

Here we examine the possibility of utilizing such a noisy nonlinear system, not just as a logic gate, but also *directly as a memory device*, i.e., we explore if the system can behave as a latch in some optimal range of noise.

A latch is a system that has two stable states and can be used to store state information. The system can be made to change state by signals applied to one or more control inputs, as shown in the truth table (Table 2). Latches are a fundamental building block of a computing machine, and is omnipresent in computers and communication systems. So proposals of implementations of a latch, that are more efficient from the point of view of space or operational time, have far-reaching consequences.

Now latches can be built around a pair of cross-coupled inverting elements, such as vacuum tubes, bipolar transistors, field effect transistors, inverters, and inverting logic gates. Specifically, for instance, conventional latches can be constructed out of two cross coupled NAND or alternately NOR gates. In present computing systems including embedded systems and other small processing units, memory access and modification time, is a significant bottleneck limiting the speed of computation.

Here, unlike traditional latches built by concatenating two logic elements, we will use only *one* element to implement the latch truth table. Our proposal does not necessitate cross-coupling logic gates, nor does it involve many clock cycles. So the direct realization of the latch here has the potential to save both space and time costs.

Specifically we will demonstrate how we can produce the Set–Reset latch operation consistently in an optimal window of noise. Namely we will show, that when the noisy bistable system is presented low amplitude input signals, consisting of two aperiodic pulses encoding two logic inputs, the output will consistently mirror a latch output (as displayed in Table 2). We also show how one can use a bias to get different types of responses from the same system, thereby obtaining an element that is easily *reconfigurable* to yield, not only gates, but a memory device as well. That is, in

* Corresponding author. Tel./fax: +91 172 2240266.
E-mail address: sudeshna@iisermohali.ac.in (S. Sinha).

0375-9601/$ – see front matter
doi:10.1016/j.physleta.2012.01.039

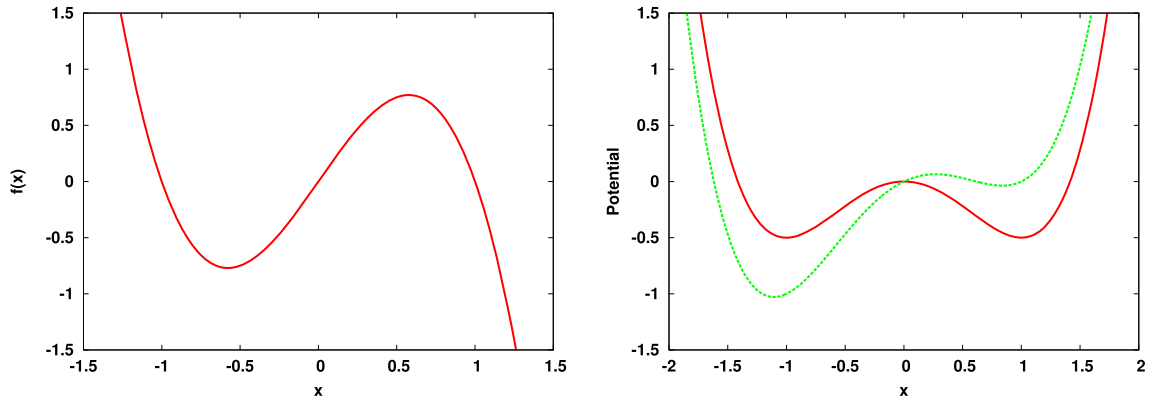

Fig. 1. For the system described by Eq. (2): (left) the function $F(x) = 2x - 2x^3$ with $b = 0$ and (right) the effective potential obtained by integrating the function $F(x)$ in Eq. (2), with bias $b = 0$ (red solid line) and $b = -0.5$ (dashed green line). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this Letter.)

an optimal range of noise, by varying the bias, the *same* system will yield logic functions like AND, OR, etc. as well as give latch operations directly.

2. General principle

Consider the general nonlinear system,

$$\dot{x} = F(x) + b + I_{in} + D\eta(t) \tag{1}$$

where $F(x)$ is a generic nonlinear function obtained via the negative gradient of a potential with two distinct stable wells. I_{in} is the input signal which encodes the logic inputs, b is bias to asymmetrize the two potential wells, and $\eta(t)$ is an additive zero-mean Gaussian noise with unit variance, with D being the amplitude (intensity) of the noise.

A logical input–output can be obtained by driving the system with two trains of aperiodic square pulses: $I_1 + I_2$, encoding the two logic inputs. For logic operations such as OR/NOR and AND/NAND, we consider the inputs to take value I when the logic input is 1, and value $-I$ when the logic input is 0, where input strength I is: $0 < I < 1$. Since, the binary logic inputs can be either 0 or 1, they produce 4 sets of binary input: $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$. These four input conditions give rise to three distinct values of I_{in}. Hence, the input signal I_{in} generated, is a 3-level aperiodic wave form.

The state of this system, can be interpreted as logic output 1 when $x > x^*$ and logic output 0 when $x < x^*$, where x^* is roughly given by the position of the barrier between the two wells. Such an interpretation allows one to consistently obtain logical responses, such as OR and AND, when noise intensity D is in an optimal band. Complementary gates, NOR and NAND, can also be obtained in a straight-forward manner, by the alternate output determination: $x < x^*$ corresponding to logic output 1, and 0 otherwise.

Now, to use this element as a Set–Reset latch, we need to modify the encoding of input values, so that we can distinguish between $(0, 1)$ and $(1, 0)$ states, as the latch truth table is *asymmetric* with respect to inputs unlike the usual logic gates. A simple way to accomplish this is to have the following asymmetric input encoding: the first input I_1 takes the value $-I$ when the logic input is 0 and I when the logic input is 1, while the second input I_2 takes the value I when the logic input is 0 and $-I$ when the logic input is 1, where $0 < I < 1$.

Equivalently, instead of the asymmetric input association described above, we can consider symmetric input associations (as in the logic operations), and apply a NOT operation to the second input I_2. This will also yield the same physical input signal I_{in}. Namely, corresponding to the 4 sets of binary inputs (I_1, I_2): $(0, 0)$, $(0, 1)$, $(1, 0)$, $(1, 1)$, the input signal I_{in} takes the values 0, -1, 1, and 0 respectively. Out of these four sets, the input corresponding to $(1, 1)$ is a restricted set and does not occur in the truth table. So we are left with three input sets, each one giving rise to a *distinct* value of I_{in}. Hence the input signal I_{in} generated, is again a 3-level aperiodic wave form.

Table 1
Relationship between the two logic inputs and the output of the fundamental OR, AND, NOR and NAND logic operations. The four distinct possible input sets $(0, 0)$, $(0, 1)$, $(1, 0)$ and $(1, 1)$ reduce to three conditions, as $(0, 1)$ and $(1, 0)$ are symmetric. Note that *any* logical circuit can be constructed by combining the NOR (or the NAND) gates [11].

Logic inputs	OR	AND	NOR	NAND
0, 0	0	0	1	1
0, 1	1	0	0	1
1, 0	1	0	0	1
1, 1	1	1	0	0

Table 2
Relationship between the two inputs and the output of Set–Reset latch.

Set (I_1)	Reset (I_2)	Latch
0	0	No change (maintain the previous state)
0	1	0
1	0	1
1	1	Restricted set

Logic response from output can be obtained, as in logic operations, by defining a threshold value x^*. If $x > x^*$, i.e., when the system is in the potential well x_+, then the logic output is taken to be 1, and 0, if $x < x^*$ and the system is in other well. Thus, the logic output toggles as the state of the system switches from one well to another.

3. Explicit example

We now explicitly demonstrate latch functionality, using a simple nonlinear system:

$$\dot{x} = 2x - 2x^3 + b + I_{in} + D\eta(t) \tag{2}$$

where D is amplitude of the Gaussian noise, b is asymmetrizing bias and the potential energy function is bistable (see Fig. 1). The input signal, $I_{in} = I_1 + I_2$, where I_1 and I_2 encode the two logic inputs, with the encoding associations for the logic operations and the Set–Reset latch being different. The bias b, for different operations, is set as displayed in Table 3.

Also note that the nonlinear function above, is efficiently realized by a linear resistor, linear capacitor, and a small number of