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Embedded Linux platform for data acquisition systems

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HIGHLIGHTS

- The design and the development of data acquisition system on FPGA based reconfigurable hardware platform.
- Embedded Linux configuration and compilation for FPGA based systems.
- Hardware logic IP core and its Linux device driver development for the external peripheral to interface it with the FPGA based system.

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ABSTRACT

This scalable hardware–software system is designed and developed to explore the emerging open standards for data acquisition requirement of Tokamak experiments. To address the future need for a scalable data acquisition and control system for fusion experiments, we have explored the capability of software platform using Open Source Embedded Linux Operating System on a programmable hardware platform such as FPGA. The idea was to identify the platform which can be customizable, flexible and scalable to support the data acquisition system requirements. To do this, we have selected FPGA based reconfigurable and scalable hardware platform to design the system with Embedded Linux based operating system for flexibility in software development and Gigabit Ethernet interface for high speed data transactions. The proposed hardware–software platform using FPGA and Embedded Linux OS offers a single chip solution with processor, peripherals such ADC interface controller, Gigabit Ethernet controller, memory controller amongst other peripherals. The Embedded Linux platform for data acquisition is implemented and tested on a Virtex-5 FXT FPGA ML507 which has PowerPC 440 (PPC440) [2] hard block on FPGA. For this work, we have used the Linux Kernel version 2.6.34 with BSP support for the ML507 platform. It is downloaded from the Xilinx [1] GIT server. Cross-compiler tool chain is created using the Buildroot scripts. The Linux Kernel and Root File System are configured and compiled using the cross-tools to support the hardware platform. The Analog to Digital Converter (ADC) IO module is designed and interfaced with the ML507 through Xilinx Generic Interface (XGI) expansion headers. The Custom IP Core is designed and implemented in FPGA to interface the external ADC with DMA engine of the on-chip processor block. The data acquisition from ADC interface is successfully achieved and the captured data is sent to the host PC on mounted NFS share (Network File System) through LAN (Local Area Network). The detailed hardware and software design, development and testing results will be discussed in the paper.

1. Introduction

The Tokamak is one of several types of magnetic confinement devices, and is one of the most-researched candidates for producing controlled thermonuclear fusion power. The need for higher throughput and scalable solutions for data acquisitions are one of the key requirements for Tokamak experiments. The number of nodes and throughput for data acquisition will continue to increase with incrementing duration of successful electromagnetic confinement at multiple phases of experimentation.

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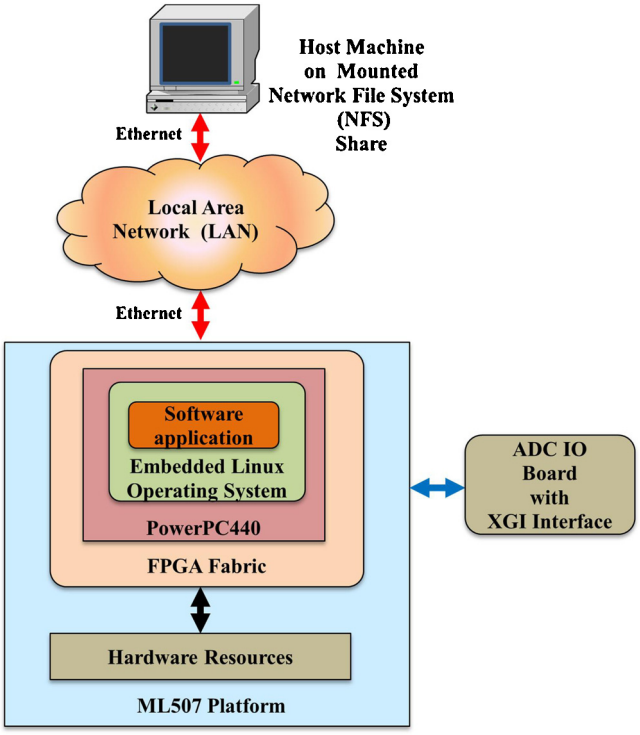

Fig. 1. Embedded Linux platform for data acquisition systems.

The work consists of development of hardware and software platform built on Xilinx FPGA with PowerPC 440 processor. The Embedded Linux platform for data acquisition is implemented and tested on a Xilinx ML507 board. The board consists of Virtex-5 FPGA, which has on-chip PowerPC 440 (PPC440) processor as a hard block. The Analog to Digital Converter (ADC) IO module with 12 bit with 2 channels is designed and interfaced with the ML507 through Xilinx Generic Interface (XGI) expansion headers, which are routed to the FPGA IO pins on the board. The board contains all other necessary IO peripherals, which are required to implement the data acquisition system. Section 2 will discussion more on the hardware platform.

The Linux Kernel version 2.6.34 with BSP support for the ML507 platform is used in this work. It is downloaded from the Xilinx [1] GIT server. Cross-compiler tool chain is created using the Buildroot scripts. The Linux Kernel and Root File System are configured and compiled using the cross-tools to support the Hardware Platform. The Custom IP Core is designed and implemented in FPGA to interface the external ADC with DMA engine of the on-chip processor block. Each DMA port is configured to handle eight channels ADC at 1 M samples/s. The data acquisition from ADC interface is successfully achieved and the captured data is sent to the host computer on mounted NFS share (Network File System) through LAN. The overall system level diagram is shown in Fig. 1. The detailed hardware design and its implementation are described in Section 2. Section 3 will discuss more on the software platform.

2. Hardware

2.1. ML507 evaluation platform

ML507 is consists of Virtex-5 XC5VFX70T device, which contains an embedded PowerPC 440 processor block with integrated DMA engines and a multi-port crossbar switch. ML507 platform is very flexible and scalable option for designers to develop high throughput solutions. The different hardware resources of ML507 platform, which are interfaced to Vitex-5 FPGA are shown in Fig. 2.

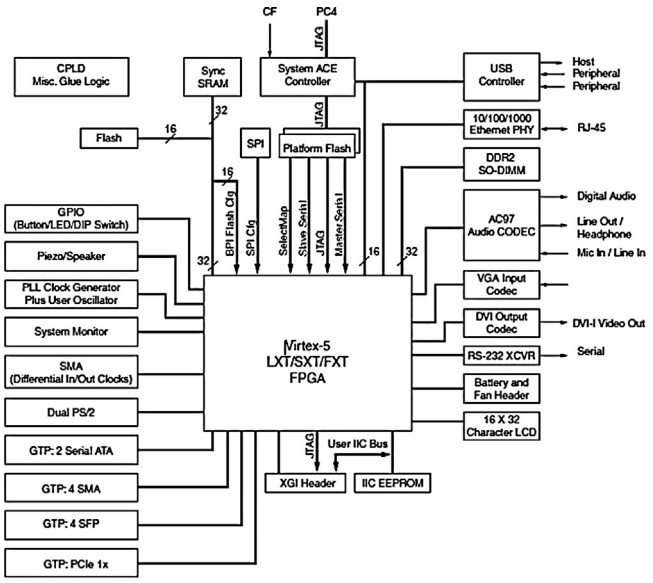

Fig. 2. ML507 platform hardware resources.

2.2. FPGA interface

The hardware resources used for the development of data acquisition system and its control and data interface with on board FPGA is shown in Fig. 3. The FPGA boundaries with other system components and its port interface with the FPGA are specified. The ADC I/O interface is an external hardware module connected though XGI interface of the ML507 platform. This system uses the PowerPC 440 (PPC440) processor block with a processor frequency of 125 MHz. The PPC440 is interfaced with different system components, i.e. DDR2 memory, Ethernet physical layer, I2C EEPROM, flash memory, universal serial asynchronous receiver/transmitter (UART), general purpose input/ouput ports (GPIO), interrupt controller and external analog to digital input/output controller (ADCIOCTRL). This hardware resources are interfaced with FPGA using Xilinx provided soft IP cores, i.e. PPC440MC DDR2, XPS BRAM, XPS MCH EMC, XPS IIC, XPS LL TEMAC, XPS UART16550, XPS GPIO, XPS INTC. The slave Processor Local Bus (SPLB) of all IP cores are connected to the master PLB (MPLB) interface of PPC440 block through PLB v4.6 bus instance. The Custom IP Core is developed for the external ADCIOCTRL, which captures and stores the data from two external ADC devices. The IP core has a slave side Processor Local Bus (PLB) interface and a Xilinx Local Link (XLL) Interface. The PPC440 uses the PLB interface for control the operations and on the other side the IP core connects to the DMA interface of the processor block through XLL interface. The Local Link Interfaces of XPS LL TEMAC and ADCIOCTRL are connected to the first and second direct memory access (DMA) port of PPC440 block respectively. The clock speed of MPLB and the DMA ports of the crossbar is set to 125 MHz.

2.3. PowerPC 440 processor

The PowerPC 440 was the first PowerPC core from IBM to include the Book E extension to the PowerPC specification. It also included the CoreConnect bus technology, which is the main interface between different parts inside a PowerPC based system-on-a-chip (SoC) device. It is a high performance core with separate 32 kB instruction and data L1 caches, a seven-stage pipeline, supporting speeds up to 800 MHz and L2 cache up to 256 kB. The core lacks a floating point unit (FPU) but it has an associated four-stage FPU that can be included using the APU (Auxiliary Processing Unit) interface. The 440 core adheres to the current Power ISA v.2.03