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EPICS based low-level radio frequency control system in LIPAc

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HIGHLIGHTS

- The system proposed can control amplitude and phase of each cavity.
- Rapid diagnostics are refreshed in milliseconds.
- Increasing control parameters will not increase consumed time neither complexity.
- IQ demodulation can be achieved thanks to the transformed values at driver level.

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ABSTRACT

The IFMIF–EVEDA (International Fusion Materials Irradiation Facility – Engineering Validation and Engineering Design Activity) linear accelerator, known as Linear IFMIF Prototype Accelerator (LIPAc), will be a 9 MeV, 125 mA continuous wave (CW) deuteron accelerator prototype to validate the technical options of the accelerator design for IFMIF. The primary mission of such facility is to test and verify materials performance when subjected to extensive neutron irradiation of the type encountered in a fusion reactor to prepare for the design, construction, licensing and safe operation of a fusion demonstration reactor (DEMO). The radio frequency (RF) power system of IFMIF–EVEDA consists of 18 RF chains working at 175 MHz with three amplification stages each. The low-level radio frequency (LLRF) controls the amplitude and phase of the signal to be synchronized with the beam and it also controls the resonance frequency of the cavities. The system is based on a commercial compact peripheral component interconnect (cPCI) field programmable gate array (FPGA) board, provided by Lyrtech and controlled by a Windows host PC. For this purpose, it is mandatory to communicate the cPCI FPGA board from EPICS Channel Access [1]. A software architecture on EPICS framework in order to control and monitor the LLRF system is presented.

1. Introduction

Paper is organized as follows: firstly the introduction. The second section, system architecture, consists of a description of the hardware and software components and a discussion of the synchrony. System operation, which describes the behavior of some parameters, some system functionalities, initialization of the IOC and the user interface, is located in the third section. The paper ends with a summary and future work exposure.

The RF system is defined as the equipment necessary to convert the high-voltage alternating current (AC) primary power to suitably conditioned RF power for input to the LIPAc accelerator cavities [2]. The quality of the RF delivered to the accelerator cavities is controlled to within ±1 degree in phase and to within ±1% in amplitude, using a low-level RF-drive modulated control system. Each RF module local control system (RF module-LCS) is a device that will monitor and control all physical parameters within the RF chains located in the same RF module. Each RF module comprises 2 RF chains, so the 18 RF chains will be monitored and controlled by 9 RF module-LCS connected via Ethernet to the central control system (CCS) [3]. This local control system (LCS) scheme is shown in Fig. 1. The primary role of the low level radio frequency system is to monitor and control the amplitude and the phase of each cavity voltage (fast regulation) and to control the tuning of each cavity to keep its resonant frequency constant. For doing so, the LLRF will generate the RF signals (RF drives) for the amplifiers feeding the cavities, depending on their voltage and forward power. LIPAc LLRF system has to work under both the CW mode operation and the pulse mode operation (during the commissioning and tuning of the prototype accelerator) [3].

The main element of the LIPAc LLRF system is based on a high performance and commercial Lyrtech FPGA VHS-ADC board for fast control that is installed in the cPCI bus of a Windows host computer. The Virtex-4 FPGA of the VHS-ADC/DAC allows us to fulfill

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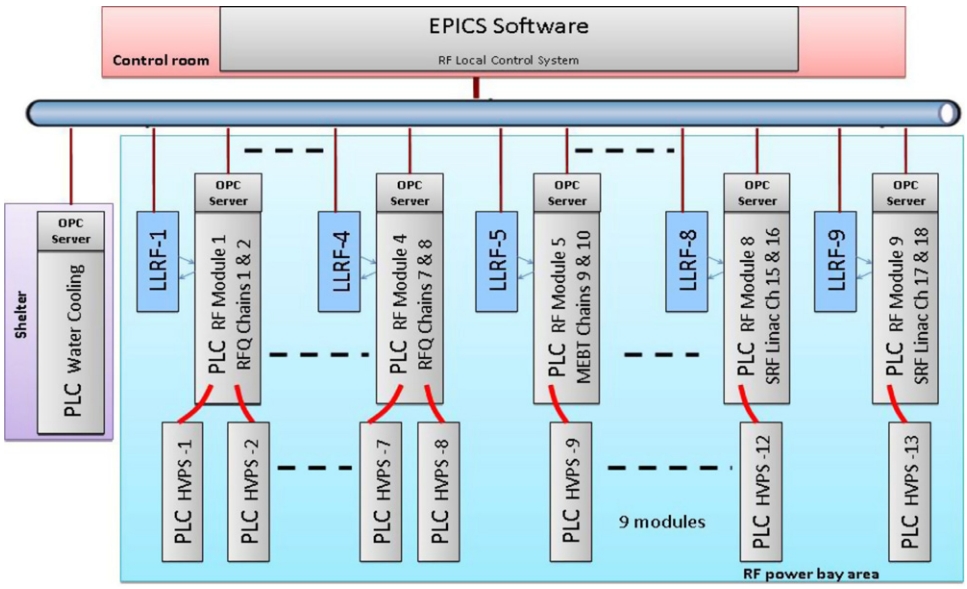

Fig. 1. LLRF local control system scheme.

our highest processing needs. If an interlock happens, FPGA card is able to make an emergency stop in less than 10 μs and it stops sending RF power to the cavities. The Virtex-4 provides us a very good logic, with one of the highest performance and density, and the memory capacity allows us to make accuracy Fast Data Logger, this FPGA board consumes only half the power needed by other FPGA families. There are two Lyrtech FPGA cards per RF module-LCS, one is called Loops and other Diagnostics. One is in charge of the amplitude, phase and tuning loops (Loops board) another one is in charge of the fast interlocks management and ancillary diagnostics (Diagnostics board). This paper presents a device support for LIPAc LLRF system, managing different applications related to control and monitor processes and data logging. Mainly, this device support is in charge of sending the parameters set by the operator to the Lyrtech board in order to modify its configuration. Communication from the device support to the board is through a bank of registers.

The application interface (API) that comes with these boards only runs under Windows operating system. Nevertheless, within the LIPAc project and for historical reasons, main control system is based on Linux OS and EPICS [4] as the main tool for the development of the control systems. Successful examples of the use of EPICS within the environment of control systems for fusion experiments can be found here [5,6]. Therefore we could consider this local system has significant differences from the model used for the main control system for the LIPAc project. Consequently, another important objective of this work is to allow a distributed control system, developing EPICS device support on the host computer and permitting the use of a different operating system thanks to properties of EPICS Channel Access.

Some examples of RF systems with EPICS can be found in [7–9]. A solution based on a digital LLRF with the same commercial board using EPICS with a JAVA IOC can be found in [10]. The work presented here has significantly more functionality than that presented in [10], such as the Fast Interlock Module, DACs and ADCs gain, system tuning, clock, VCXO programming or Fast Data Logger. In addition, there is a fundamental difference between our work and [10], namely what we present to the final user is an interface where all internal processes related to control and monitoring are transparent. In contrast, the work presented in [10], includes some tools which require programming and configuration by the final user. Thus, the work presented here is novel because no solutions in the literature have been found with the features and functionality of our software architecture for an LLRF system.

This work is based on the first paper published in [1]. The main contribution with respect to this first work is related to the description of the system architecture and the system operation, which becomes one of the fundamental cores of the control system.

2. System architecture

2.1. Hardware architecture

The LLRF system is composed by three main subsystems: a digital board with fast FPGA, the analog front end and a local timing system. It is a similar scheme as [11].

- Digital board: The digital board contains one Virtex-4 FPGA, 8 ADCs and 8 DACs with 14 bits resolution and capable to work up to 105 MHz. It is a commercial board with cPCI format provided by Lyrtech and controlled by a Windows CPU. This board acquires different kind of signals: RF control inputs (cavity voltage and forward cavity power), RF interlock inputs, digital interlocks and timing signals (gate and pulse signals). It also provides the control outputs of the LLRF: DC signals to be modulated into RF to control amplitude and phase of cavity voltage, interlock output to open a pin diode switch to stop the RF when an interlock happens and low voltage transistor-transistor logic (LVTTL) pulses to move a motor that adjusts the resonance frequency of the cavity. The cavity interlocks inputs controlled by the LLRF are: *reflected power of the cavity, vacuum pressure, arcs* and *multipacting*. Furthermore, the Machine Protection System (MPS) will be also connected to the Fast Interlock utility of the LLRF to switch off the RF Drive when required. A scheme of a LLRF module is shown in Fig. 2.
- The front end: This is in charge of up-converting the DC control outputs from the digital board into RF. For doing so, the LLRF employs a quadrature IQ modulator.
- The local timing system: It consists of a PLL board with a 100 MHz VCXO (CDC-7005-EVM from Texas Instruments). This board provides 100 MHz TTL signal to clock the digital board. This signal